5. Bistability and Cascadable Logic Inversion in a 1550 nm VCSEL

An underlying assumption throughout this thesis is that the optical transmission channel is linear. That is to say, the signal input/output (I/O) relationship can be conveniently modeled using linear operators. Thus, propagation and filtering effects are easily represented, for example, by invoking the principle of convolution. More importantly, the accumulation of noise has been assumed to obey superposition laws in the sense that the total noise in the system is modeled by the independent summation of independent noise sources. This assumption does not hold for a variety of situations. For example, if the launched power into the fiber increases above a certain threshold, certain nonlinearities such as SPM, XPM, FPM, SBS and stimulate Raman scattering (SRS) will begin to impair signal propagation [1, 2]. The prediction and modeling of these complex photonic interactions requires sophisticated techniques beyond the scope of this work.

Another important area where system linearity is violated is in regenerative systems. The concept of signal regeneration is implicit in modern computing. Because modern transistors possess highly nonlinear I/O characteristics, it is possible to cascade unfathomable numbers of transistors on a single chip without incurring bit errors. This immense computing capability is made possible by the fact that the

transistors inhibit electrical noise accumulation through the process of signal regeneration. Therefore, the nonlinear response of the system to noise guarantees error-free operation for the entire lifetime of the chip [3]. Because optics cannot provide commensurate processing power, it is no wonder that the processing core of modern optical networks continues to reside in the OEO network nodes where electronic hardware provides all necessary routing intelligence.

These facts motivate several important questions: Is it possible to circumvent *electronic* signal processing in optical data networks and replace it with *optical* signal processing? Can the intelligence of the network reside in the optical domain? Which technologies, if any, provide the necessary regenerative aspects of digital computing such that all optical signal processing can be realized? Although the inevitable progress of photonics technology promises that optical information processing (OIP) will one day replace the costly and burdensome electronics in optical networks, the means by which to make this possible is yet unclear.

In this chapter, it is demonstrated that 1550 nm VCSEL technology may be a promising candidate for future OIP systems. While VCSEL technology has been extensively studied previously for OIP applications in the 850 nm wavelength band, the work in this chapter describes recent advancements in 1550 nm VCSEL OIP technology. The nonlinear characteristics of 1550 nm VCSELs are studied and novel nonlinear responses are measured for the first time. The nonlinear behavior of the device is then utilized to build a fully cascadable all optical inverter. These

experimental demonstrations represent the first major steps in the devlopment of 1550 nm VCSEL technology for OIP applications.

5.1 Bistability in 1550 nm VCSELs

5.1.1 Introduction

All-optical Boolean logic has been a heavily researched topic for several decades due to its potential impact in OIP including areas such as optical signal processing (OSP), optical computing, and optical packet switching [4-6]. Although a multitude of techniques exist which achieve OIP including XGM and XPM in semiconductor optical amplifiers (SOA) [7], four wave mixing (FWM) in highly nonlinear fiber [8], intensity bistability in Fabry-Perot laser amplifiers (FPLA) [9, 10] and polarization bistability in VCSEL [11], no clear technology candidate has emerged for large-scale OIP because of shortcomings in terms of speed, power, size, large scale integrability and cost of logic elements. Over recent years, intensity bistable VCSOAs[1] have received interest for applications in OSP at 850 nm [12-16]. Owing to their gain and highly nonlinear resonant structure, 850 nm VCSOAs have been shown to achieve critical functionalities such as re-amplification and reshaping (2R) [13], optical inversion [17], self-sustained ring oscillation [18] and optical flip-flop [19, 20] Most importantly, as a mature technology platform, 850 nm VCSOAs offer an excellent tradeoff in terms of speed, power, size, integrability, and cost. Contrastingly, work in 1550 nm VCSOAs is still nascent as a result of the greater

[1] A VCSOA is a VCSEL which is biased below threshold in order to be used as a resonant optical amplifier.

difficulty in fabricating 1550 nm VCSELs. Nevertheless, VCSEL/VCSOA research is ongoing in the telecom band for its potential economic impact [21].

Recently, Hurtado *et al*. [22] observed optical bistability in 1550 nm VCSOAs. The operating conditions necessary to achieve bistable switching were stringent with large switching power of 150 μW for counterclockwise and 600 μW for clockwise bistability. The narrow operating range is explained, among other factors, by the large insertion loss (20 dB) suffered when coupling into and out of the device. In order to compete with alternative technologies and to justify the use of bistable VCSOAs in commercial telecom applications, the switching power must be reduced. In this section, optical bistability is experimentally observed using commercially available, fiber pigtailed 1550 nm VCSOAs with switching powers as low as 2 μW, two orders of magnitude smaller than previously reported and comparable to that of 850 nm devices. Moreover, it is observed for the first that VCSOAs exhibit *all three* types of bistability: counterclockwise, clockwise, and butterfly. A physically intuitive explanation for the existence of the various forms of bistablity in reflection mode VCSOAs is developed. All three types of bistability are observed experimentally by changing either the current bias of the device or the injected wavelength into the device. It is found that optical bistability is readily achievable for a wide range of bias currents and wavelength detuning. These results help substantiate the claim that VCSOAs can be a key technology for future OIP applications at 1550 nm.

5.1.2 Theory

Optical bistability is the ability of a device to operate in two stable states, depending on the input history. When light is injected into the active resonant cavity carriers are consumed, resulting in gain through the process of stimulated emission. The accompanying drop in the carrier concentration leads to an increase in the refractive index of the cavity. This refractive index change, in turn, leads to a red-shift in the peak resonant wavelength of the cavity. When the injected light is detuned toward the long wavelength side of the gain window, carrier depletion shifts the cavity resonance toward the injected wavelength causing positive feedback. The combination of this dispersive non-linearity and gain saturation within the cavity leads to a counterclockwise bistability in the *transmitted* intensity [6].

Whereas *transmission mode* devices only exhibit counterclockwise bistability, it has been known for some time that dispersive bistable laser diodes operated in *reflection mode* also exhibit two additional forms of bistability known as butterfly and clockwise bistability [4, 10]. *Butterfly and clockwise bistability are manifested through the careful balance between the incoming and outgoing intensities in the laser amplifier cavity* [4, 9, 10, 22, 23].

Physical insight into the existence of butterfly and clockwise bistability is gained when one considers that, in steady state, incoming and outgoing intensities must equate [9] as described by:

$$I_{ref} = I_{in} + gL \cdot I_{av} - I_{trans}. \tag{5.1}$$

here I_{in} is the input intensity, I_{av} is the average intensity inside the cavity, gL is the single pass gain, and I_{trans} is the transmitted intensity. Effectively, the total intensity outside the cavity through I_{ref} and I_{trans} must equal the total intensity inside the cavity (I_{in} and $gL*I_{av}$). As stated above, dispersive nonlinearity and gain saturation always combine to cause counterclockwise bistability for I_{trans}. Since I_{in} is a linear term, the behavior of I_{ref} can ultimately be understood by determining $gL*I_{av}$ and solving (5.1).

Solutions to (5.1) are illustrated in Fig. 5.1 to demonstrate how both counterclockwise and clockwise bistability can arise by making the simple assumption that $gL*I_{av}$ exhibits counterclockwise bistability. Physical insight into this complex balancing of the terms in (5.1) can be garnered when one considers two extremes of operation: first when the current bias is high (e.g. ~99% of threshold) and the wavelength detuning is small and second when current bias is reduced (e.g. ~90% of threshold) and wavelength detuning is large. As depicted by the solid lines in Fig. 5.1, at high values of bias and low values of detuning, the second term in (5.1) dominates due to larger gain, and the reflected intensity, I_{ref}, mimics the S shaped counterclockwise solution of $gL*I_{av}$. As the bias is reduced and the detuning is increased (depicted by the dotted lines), the bistable functional form of I_{trans} grows larger than $gL*I_{av}$ due to reduced gain and thus begins to dominate the right side of (5.1). By summing the S-shaped I_{trans} and $gL*I_{av}$ terms and the linear I_{in} term, Fig. 5.1 shows that I_{ref} results in a clockwise hysteresis loop (dashed black curve). During the transition region between counterclockwise and clockwise bistability, when $gL*I_{av}$ and

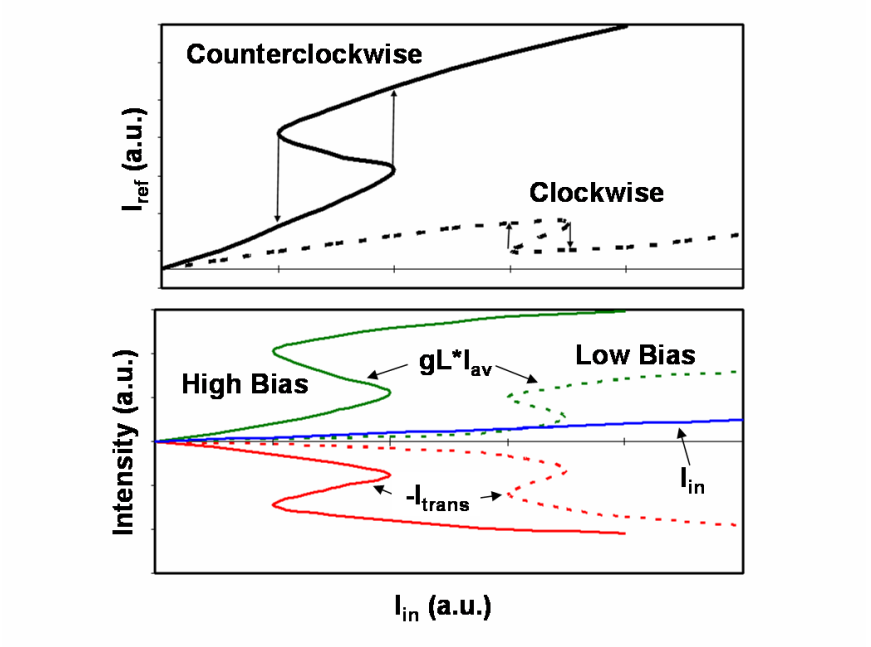


Fig. 5.1. Illustration of (5.1) explaining the existence of clockwise bistability in reflection mode VCSOAs. Solid curves represent higher bias-lower detuning case which generates counterclockwise hysteresis in I_{ref}. Dotted curves represent lower bias-higher detuning case which generates clockwise hysteresis in I_{ref}. The transition between these two regimes generates butterfly hysteresis.

I_{trans} are of comparable magnitude, I_{ref} exhibits butterfly bistability in which both discontinuous transitions fall from higher to lower powers.

It is worth noting that while I_{trans} will always exhibit counterclockwise bistability though the effects of dispersive nonlinearity and gain saturation, it is not generally true that $gL*I_{av}$ is always counterclockwise bistable. As was shown in [23], $gL*I_{av}$ can also exhibit butterfly and clockwise bistability (see Fig. 5 in [23]). Nevertheless, this fact does not distract from the physical interpretation above that it is the careful balancing of (5.1) which yields the complex bistability curves observed in the reflected intensity.

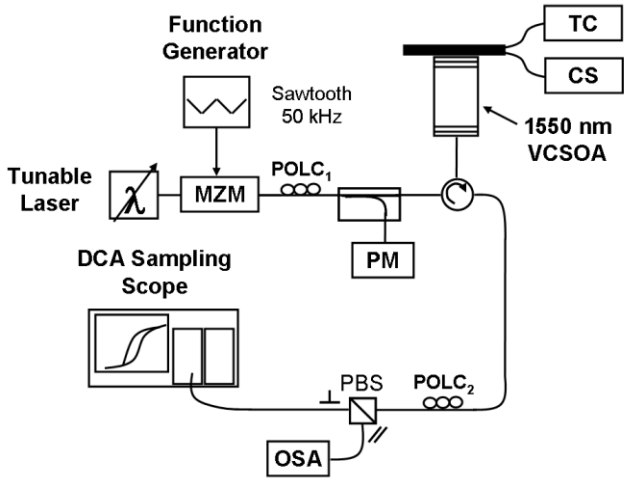


Fig. 5.2. Experimental Setup to study bistabilty in 1550 nm VCSOA.

5.1.3 Experimental Setup

The fiber-coupled experimental setup used to study the bistable switching properties of our 1550 nm devices is shown in Fig. 5.2. A single mode 1550 nm fiber pigtailed VCSEL from Raycan (Korea) was used for the demonstration. The VCSEL had a threshold current, I_{th}, of 1.99 mA, a peak gain of about 11 dB for an optical input of 1 μW at a wavelength of 1542.290 nm on the stronger gain axis, and a peak gain of about 7 dB for the weaker gain axis for an input of 1 μW and a wavelength of 1542.830 nm. The gain windows were approximately 8 GHz wide for an input of 1 μW and around 12 GHz wide for an input of 10 μW. This intensity dependent gain window bandwidth is consistent with previous work with 850 nm VCSOAs [13, 16].

Tunable laser light is first intensity modulated using a MZM driven by a 50 kHz sawtooth wave. This allows for real-time plotting of the I/O characteristics of the VCSOA by using the processing functionalities of the digital communication analyzer

(DCA) sampling scope. After the MZM, the injected light is aligned in polarization to the strong gain axis of the VCSOA via a $POLC_1$. The light is then injected into a fiber coupled 1550 nm VCSOA via a circulator. The VCSOA output is passed back through the circulator and then through $POLC_2$ and a PBS. The PBS helps facilitate polarization alignment to the stronger gain axis of the VCSOA and rejects the ASE in the polarization orthogonal to the signal. The I/O are plotted on the sampling scope. The current source (CS), temperature controller (TC), power meter and OSA are used to carefully control and monitor VCSOA bias current, I_{bias}, temperature, input optical power and polarization alignment, respectively.

5.1.4 Results

As described above, Fabry-Perot bistability theory predicts that, for a given bias current, counterclockwise bistability will onset first as the input wavelength is red-shifted with respect to the amplifiers peak resonant wavelength. Upon further detuning, the I/O characteristics will transition to butterfly and then clockwise bistability. Experimental observation of this transition can be seen Fig. 5.3. Clearly, at larger detuning butterfly and clockwise bistability can be obtained at the expense of higher switching powers and wider hysteresis windows.

In a similar fashion, the transition between all three bistable regimes can be observed if the wavelength detuning is kept constant and the bias current is swept as shown in Fig. 5.4. Physically, as the bias current is decreased, the resonant peak of the amplifier blue shifts. This effectively causes the wavelength detuning to increase

thereby resulting in butterfly and clockwise bistability. Consistent with Fig. 5.3, Fig. 5.4 shows that counterclockwise bistability has the lowest switching powers and narrowest hysteresis windows.

Since it is desirable in signal processing applications to have minimal power dissipation per gate, the next step is to find the minimum bistable switching power achievable in our device. In Fig. 5.5, counterclockwise bistability is plotted as a function of wavelength detuning for a fixed bias current of $0.99*I_{th}$. Again, as the detuning is swept towards longer wavelengths, the bistable switching power shifts towards higher values and the overall widths of the hysteresis windows increases. Most importantly, it is found that a minimum switching power of 2 μW can be obtained for a wavelength detuning of 27 pm. This minimum power is limited mainly by the internal noise floor of

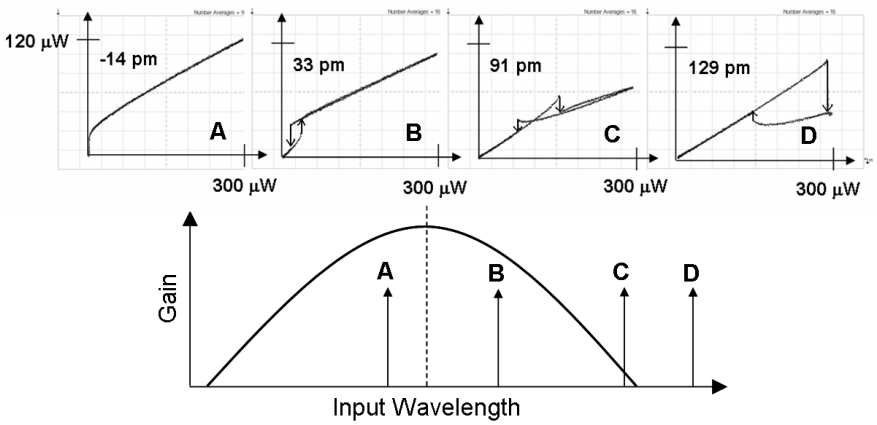


Fig. 5.3. All three types of bistability in a 1550 nm VCSOA for constant $I_{bias} = 0.96*I_{th}$. Wavelength detuning is swept towards longer wavelengths. A is for no bistability. B is counterclockwise bistability. C is butterfly bistability. D is clockwise bistability.

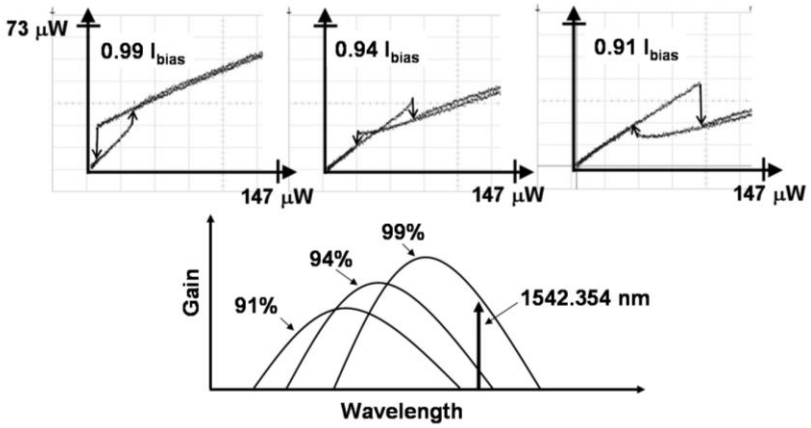


Fig. 5.4. All three types of bistability for constant wavelength 1542.354 nm . I_{th} is swept. 99% I_{bias} shows counterclockwise bistability. 94% I_{th} shows butterfly bistability. 91% I_{th} shows clockwise bistability.

the DCA detector and may be an overly conservative value. Compared to previously published results on 1550 nm VCSOA [22], 2 μW represents a two order of magnitude improvement in minimum possible switching power. This improvement is mainly attributed to the fact that the fiber pigtailed VCSOA has significantly better I/O coupling compared to the free space coupling losses present in previous studies. It is estimated that the coupling losses are about 3 dB, yielding a 17 dB improvement over that used in [22]. For this reason, it is evident that sound packaging and integration methods must be developed to minimize I/O coupling losses for future VCSOA-based OIP. This demonstrated μW level switching is readily achievable and represents an important advantage of VCSOAs over traveling wave SOA optical logic technologies based on XGM and XPM [7].

It was recently shown that polarization bistability in VCSELs can achieve switching powers on the order of 100 nW [11] for a 100 MHz switching frequency.

While such a low switching power is advantageous, it was also shown that the required switching power increased with increasing switching frequency (~80 μW peak power for 10 GHz) owing to the narrow sensitivity region of the wavelength detuning characteristics [11]. Since polarization bistabilty is also known to be susceptible to self-heating effects [24, 25], it can be argued that dispersive bistability in VCSOAs may offer a viable alternative for OIP applications. Furthermore, it is believed that a future optimization of the VCSOA device structure may further reduce the switching power to sub-μW levels.

In terms of the bistable sensitivity of our devices to operating conditions, it is found that all three forms of bistability manifest over an extremely wide range of bias currents and wavelength detuning, limited primarily by the available power in the experimental setup. This contrasts with previously reported results which showed a relatively small range of operating conditions to achieve bistable switching [22]. As it is shown in Figs. 5.5-5.7, all three forms of bistability exist over tens of pm of detuning. Moreover, the results in [22] showed very narrow hysteresis windows. This improvement is attributed to the improved coupling efficiency of these fiber pigtailed devices. Additional modeling using the technique described in [12] also indicates that the existence of bistability in VCSOAs in critically dependent on device properties such as top/bottom mirror reflectivity, linewidth enhancement factor, cavity confinement and overall gain. These factors may further explain why the tested devices exhibit much stronger bistability. The measurements show counterclockwise bistability visible from 83% I_{th} to 122% I_{th}, butterfly bistability from 81% I_{th} to 114%

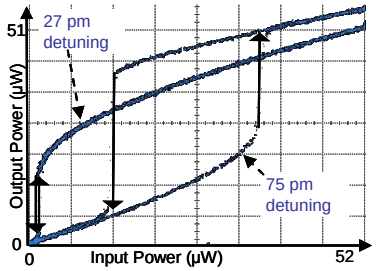


Fig. 5.5. Counterclockwise Bistability for 0.99*I_{th}.

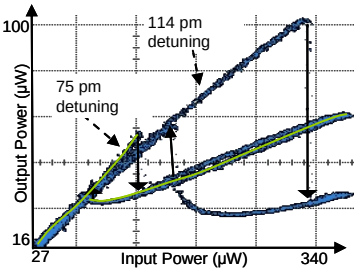


Fig. 5.6. Butterfly Bistability for 0.99*I_{th}.

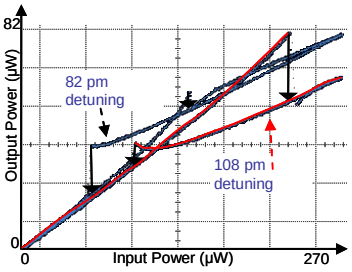


Fig. 5.7. Clockwise Bistability for 0.89*I_{th}.

I_{th}, and clockwise bistability from 66% I_{th} to 108% I_{th} where the upper end of the bistability for clockwise and butterfly bistability is limited by the available input power of the setup. Hysteresis windows as large as 119 μW (54-173 μW) for counterclockwise and 164 μW (89-253 μW) for clockwise bistability are also observed, limited only by the available input power of the system. The robustness and flexibility of these devices to exhibit bistable behavior over a wide range of operating

conditions is of practical interest for possible future applications and will be discussed further in Section 5.2.

5.1.5 Conclusion

This section has dealt with the first ever observation of all three types of bistability in VCSOAs. It has been shown that the onset of bistable action occurs at thresholds as low as 2 μW which is more than two orders of magnitude smaller than any previously reported observation in 1550 nm VCSOAs. The significance of achieving low switching thresholds is of practical concern for applications in all-optical signal processing. It has also been shown that all three forms of bistability occur over a wide range of operating conditions indicating that these devices may offer great flexibility for future applications.

5.2 Cascadable 1550 nm VCSEL Inverter

5.2.1 Introduction

From Section 5.1, it was rigorously demonstrated that commercially available 1550 nm VCSELs can exhibit large nonlinear responses. While the observation of all three forms of reflective bistability is scientifically interesting from a device perspective, the ultimate goal is to use these devices for practical, optical computing purposes. In particular, it is important to describe and predict how a single VCSEL logic element might behave in a larger system.

In order to build towards this greater goal of large scale optical signal processing systems, it must first be proven that 1550 nm VCSEL technology can be used as a fundamental building block in an actual communications setup. In this

section, the large nonlinearity of the VCSELs is exploited to create the fundamental building block of all digital communications (electrical or optical): the inverter[2]. optical processing logic.

A critical, and often overlooked, impediment towards the large-scale development of OIP systems is the necessity for cascadable operation. A logic gate is said to be cascadable as long as it satisfies two criteria: first that it possesses an input/output transfer characteristic (TC) with *positive noise margins* (NM), and second that it can provide *logic level regeneration* [26]. The requirement of positive noise margins ensures that unwanted noise fluctuations do not cause logic level errors between consecutive logic elements. The second requirement, that the gate can provide signal regeneration, ensures that any pathological signal will converge back to a stable operating point after propagation through several gate elements. Provided that these two necessary conditions are met, it is possible to then analyze the overall *noise immunity* to determine the systems ability to operate error-free in the presence of all available noise sources [3]. The concept of noise immunity specifically refers to system level considerations and is beyond the scope of this study.

The primary goal of Section 5.2 is to demonstrate the feasibility of a novel optical inverter gate based on 1550 nm VCSEL technology which simultaneously achieves positive NM and logic regeneration. The proposed scheme takes advantage of XGM and dispersive bistability [27] in an injection locked 1550 nm VCSEL. A discussion the operating principle behind the inverter is offered and measurements of

[2] An inverter performs the Boolean "NOT" operation. Thus, an input HIGH becomes and output LOW and an input LOW becomes an output HIGH.

noise margin (NM), frequency response and output extinction ratio (ER) reveal that positive NM and ER regeneration are possible up to 2.5 Gb/s using a *commercially available, non-optimized device*. BER measurements confirm that error-less performance can be achieved with sensitivity penalties of 0 and 1.4 dB for 1 Gb/s and 2.5 Gb/s inversion, respectively. The various design and optimization tradeoffs are discussed along with future implications towards the realization of OIP systems using VCSOA/VCSEL logic technology.

5.2.2 Principle of Operation

At a given bias current, a VCSEL typically lases in a linear polarization determined by the crystal axes of the semiconductor. Birefringence splits the emission frequencies of the two polarizations, and one polarization (the lasing polarization, or LP) typically dominates as depicted in Fig. 5.8a [28]. Although light emission in the linearly polarized orthogonal fundamental transverse mode (deemed the orthogonal polarization, or OP) is suppressed, external light injected into the OP gain window can be amplified. Pan *et al*. showed that the output polarization can be bistably switched to the OP if OP light is injected into the VCSEL cavity [29]. Use is made of this polarization switching for inversion as shown in Fig. 5.8b and Fig. 5.8c. First, CW light is injected into OP as depicted in Fig. 5.8b. Under this condition, the VCSEL injection locks to the OP mode and the LP mode is suppressed. The injection of OP light serves two purposes: the injected light biases the device near the switching point between the two polarization modes and the increased photon density decreases the carrier recombination lifetime.

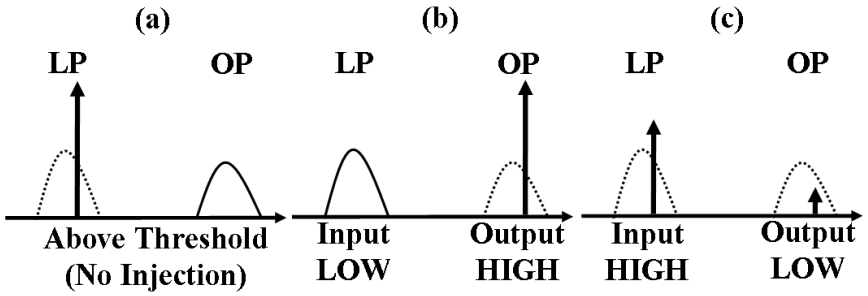


Fig. 5.8. Principle of operation for an above threshold VCSEL inverter. (a) Under no external injection (i.e. free-running), the VCSEL lases in LP mode and the OP region acts as a gain window. (b) CW light injection locks the VCSEL to the OP mode, similar to that described in [29]. (c) The output power of the injection locked OP mode is modulated through XGM by a second light injected into the LP gain window. The injection locked OP light varies inversely with the modulated LP signal.

The injection locked OP mode acts as the output of the inverter. When no light is injected into the LP (input = Low), the output OP light is at a maximum (output = High). However, if light is injected into the LP gain window (input = High), as shown in Fig. 5.8c, carriers are depleted within the laser gain region causing the OP light to become a logic Low. The transfer characteristic of this inverter scheme depends on the relative frequency detuning and power of the two injected fields, the bias current and the temperature.

5.2.3 Experimental Setup

To study the inverter scheme described in Fig. 5.8, a commercially available (Raycan, Korea) 1550 nm fiber pigtailed VCSEL was used. This VCSEL was similar in operation to the device studied in Section 5.1. The VCSEL had a threshold current

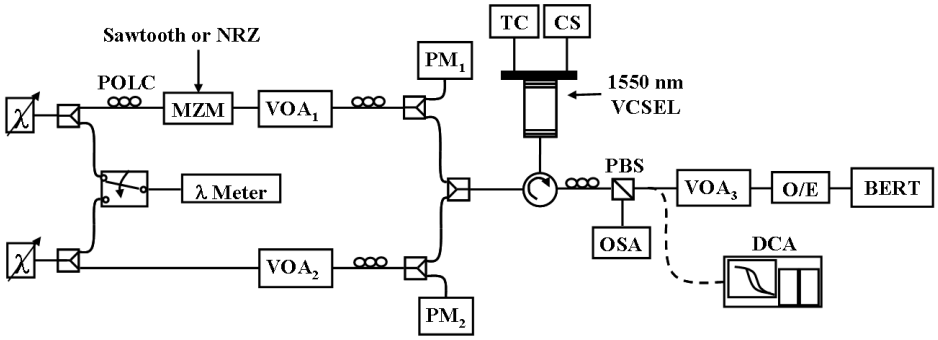


Fig. 5.9. Experimental setup to study VCSEL inverter.

(I_{th}) of 2 mA at a temperature of 21^{o}C and exhibited gain window separation of approximately 500 pm between OP and LP. The maximum small signal gain of the amplifier biased at 1.98 mA was 12 dB for the LP window and 11 dB for the OP window.

The experimental setup used to characterize the performance of the above threshold 1550 nm VCSEL inverter is described in Fig. 5.9. Two tunable lasers are used for LP and OP light injection. For convenience, the modulated LP injection light will be referred to henceforth as *signal* light or optical *signal* and the CW OP injection light will be referred to as the *bias* light or optical *bias*. The inverted output signal will be referred to as the *output* light or *output* inverted signal. The wavelengths of the lasers are carefully monitored by a wavelength meter (λ Meter). The signal light passes through a high speed Mach Zehnder modulator (MZM) modulated by either a NRZ PRBS pattern for BER measurement or a low frequency saw-tooth waveform for transfer curve measurement. The VOA, POLC, power meters (PM), PBS and OSA are used to adjust the injected powers into the LP and OP and to align the light along the principle states of polarization of the VCSEL. The injected bias current (I_{bias}) is

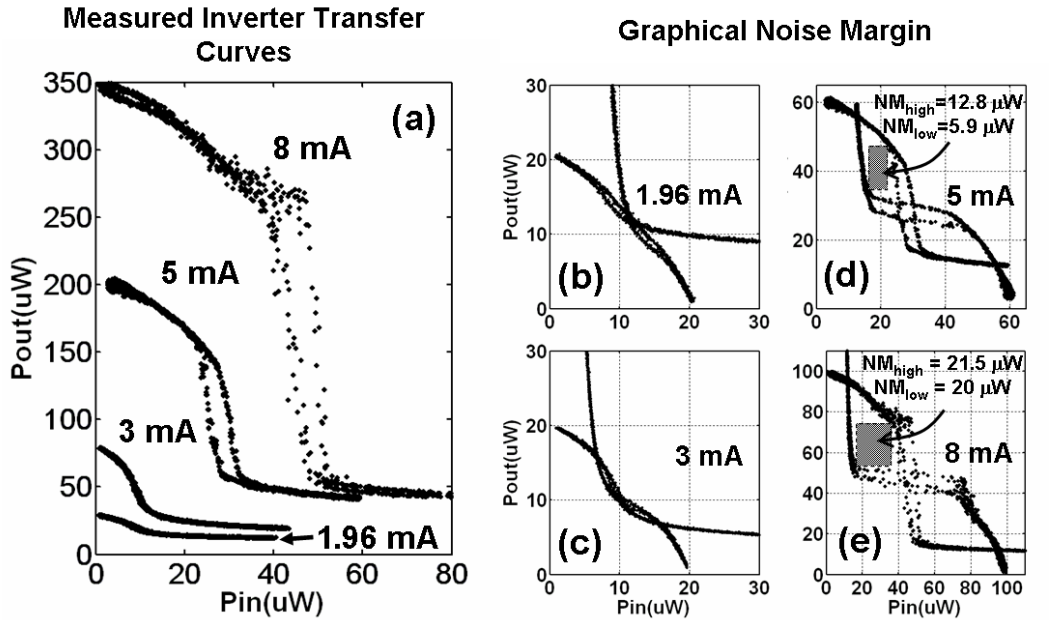


Fig. 5.10. (a) Inverter transfer curves for various bias currents. (b-e) Graphical calculation of noise margin using MPC.

adjusted with the current source (CS) and the temperature is stabilized to 21^{o}C with a temperature controller (TC in Fig. 5.9). Depending on the parameter being measured, the inverted output is either monitored on a DCA sampling scope or is passed to an optical-to-electrical receiver for BER analysis.

5.2.4 Noise Margins and the Largest Square Method

Using the saw-tooth modulation shown in Fig. 5.9 in conjunction with the real-time processing capability of the DCA sampling scope, the input-output response of the VCSEL inverter is measured. Figure 5.10a shows the inverter transfer characteristic for four bias currents. Operating conditions were experimentally determined by simultaneously maximizing output extinction ratio and minimizing injected power. The nonlinear (bistable) TC of the inverter clearly steepens as the bias

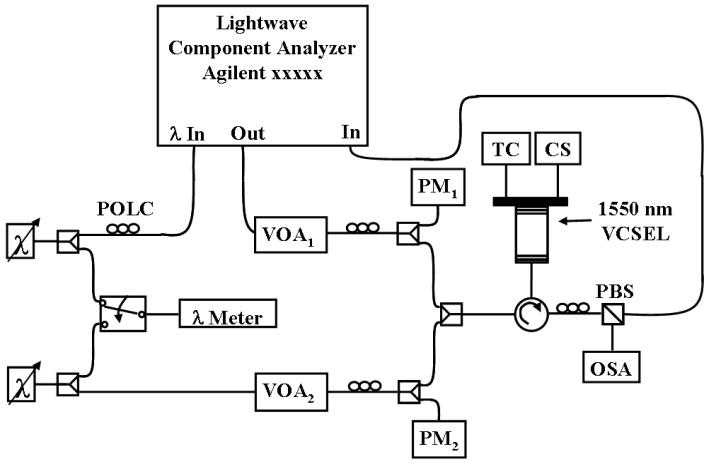
current in increased. Moreover, increasing bias current causes increased output power at the expense of higher switching power. For sufficiently high bias current, the output power exceeds the switching power and positive NM is possible. By adopting the graphical procedure in [30, 31], and scaling the vertical axis (since output High is larger than is required), Fig. 5.10b-e show the calculated NM using the maximum product criteria (MPC). Although various figures of merit have been proposed to quantify the noise margin, the maximum product criteria (MPC) is the best graphical technique for static noise margin measurements based on its applicability for many different logic families [30]. Above about $2*I_{th}$, positive NM is achieved as evident by the depicted rectangles in Fig. 5.10d and Fig. 5.10e. Below this value, the transfer characteristics do not yield closed loops meaning positive NM cannot be achieved, thereby precluding cascadability.

5.2.5 Speed

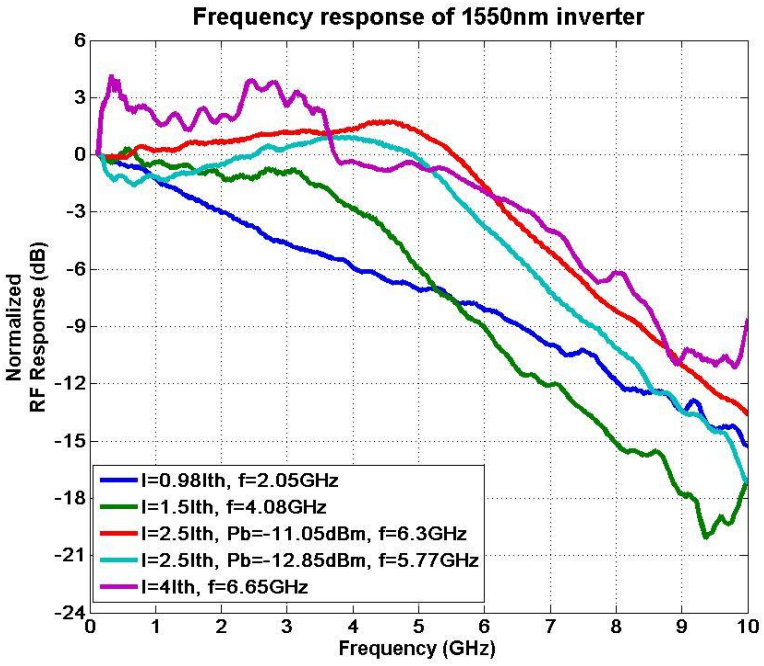
It is known that strong optical injection into a directly modulated VCSEL device results in a considerable modulation bandwidth enhancement [32]. The physical explanation for the bandwidth enhancement is that the carrier lifetime inside the laser cavity is reduced for higher optical intensities inside the cavity. Recently, it was shown that XGM in VCSOA devices are also limited by carrier lifetime effects [33]. Thus, it is reasonable that driving the VCSEL with higher bias current and/or injecting higher optical power should improve the achievable bandwidth of the inverter.

In order to study the effect of bias current and injected power on the speed of the inverter, the experimental setup was altered slightly as shown in Fig. 5.11a. For speed measurements, the MZM is replaced in Fig. 5.9 with an Agilent 8703A Lightwave Component Analyzer (LCA). The optical-optical frequency response capability was used which measured of the small signal frequency response of the inverted output signal for swept values of sinusoidally modulated input signal light. All other features of the experimental setup were the same except that the internal modulator of the LCA was used to produce the swept sinusoidal modulation. The inverted output light was then fed back into the LCA input port to measure the calibrated frequency response of the inversion process.

As is shown in Fig. 5.11b, the frequency response of the inversion process through XGM is greatly enhanced with increasing bias current and optical injection power. Below threshold, the inverter 3 dB bandwidth is 2.05 GHz. This value is consistent with the carrier lifetime-limited speed of 2.5 GHz predicted in [33]. Above threshold, higher optical intensities inside the cavity result in larger modulation bandwidths similar to directly modulated VCSELs under high optical injection. For the largest bias current measured, the inverted signal 3 dB bandwidth reached 6.65 GHz representing better than 3.5 times improvement over the below threshold inverter. Moreover, by increasing the bias power (P_{bias}) for fixed current bias, it was also possible to improve the speed of the inverter. For example, a 1.8 dB increase in optical bias power (-12.85 dBm to -11.05 dBm) increased the 3 dB bandwidth of the inverter by 530 MHz (5.77 GHz to 6.3 GHz) at a current bias of 5 mA. Unfortunately,



(a)



(b)

Fig. 5.11. (a) Experimental setup for frequency response measurement. (b) Frequency response curves for various bias currents.

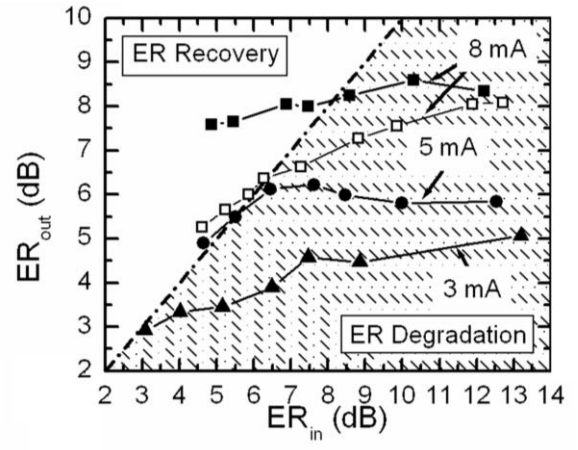


Fig. 5.12. ER regeneration for various bias currents. Points above the ER_{in} = ER_{out} boundary result in ER regeneration, points below result in ER degradation. Solid marks represent 1 Gb/s values. Empty marks represent 2.5 Gb/s values.

this faster device response must necessarily be traded for increased optical bias power. Moreover, it was found that increasing the optical bias reduced the output ER of the inverted signal. Therefore, one must be prudent when attempting to improve the frequency response with higher input powers since power and ER limitations must be considered. In general, results of Fig. 5.11b indicate that some amount of speed improvement can be expected using this inverter scheme as compared to the below threshold analog previously studied [17] .

5.2.6 Cascadability and BER

Having determined the noise margin and speed characteristics of the inverter, the regenerative properties are now verified. The regeneration property corresponds to the impact the inverter has on the ER of the input signal. In principle, if the ER_{out} is

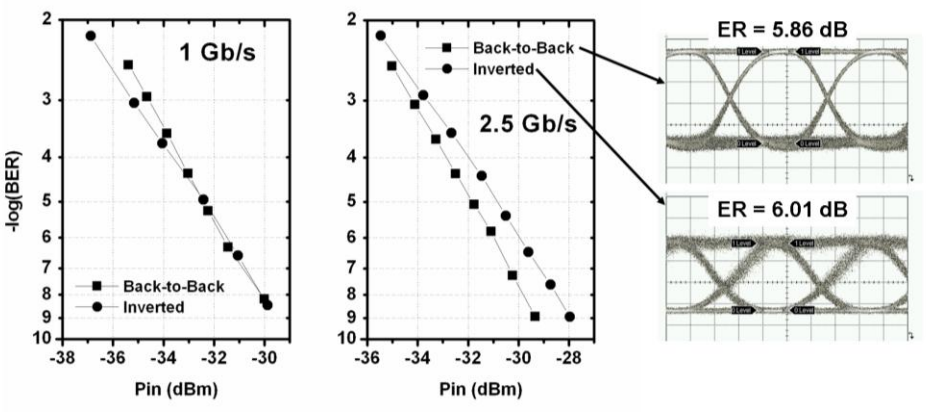


Fig. 5.13. BER curves showing input signal performance versus inverter signal performance. Accompanying eye diagrams for the 2.5 Gb/s curves demonstrating slight ER improvement.

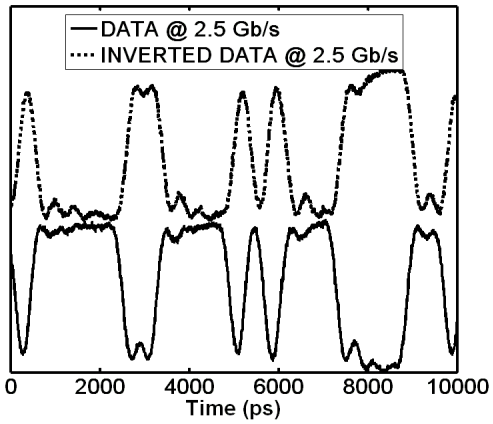


Fig. 5.14. Bit pattern showing data inversion for 2.5 Gb/s.

larger than the ER_{in}, then the gate can provide the necessary signal regeneration for any pathological signal propagating through the OSP circuit.

ER regeneration is demonstrated by plotting the inverted output extinction ratio of the device versus the ER of the input signal as shown in Fig. 5.12. It is evident that the input ER has a strong influence on the ER_{out} and only at high bias current (> 5 mA) can the ER of the inverted signal be restored. Data rate also plays an important role in the regenerative properties of the inverter. Consider the comparison between 1 Gb/s and 2.5 Gb/s signals for the 8 mA bias current. At 1 Gb/s (solid

squares) ER regeneration is possible whenever ER_{in} < 8dB. At 2.5 Gb/s (empty squares), the ER_{out} is only marginally improved for ER_{in} < 6 dB. This data rate dependence is caused by the finite response time of the device and limits cascadable operation above 2.5 Gb/s with the VCSELs used in this experiment.

Finally, the BER of the inverted signal compared to the input signal under conditions where the $ER_{out} > ER_{in}$ is measured. The results for 1 Gb/s and 2.5 Gb/s are shown in Fig. 5.13 with the accompanying inverted bit pattern at 2.5 Gb/s in Fig. 5.14. As would be expected, the inverted 1 Gb/s signal does not suffer a sensitivity penalty because the penalty associated with the filtering effects of the VCSEL is offset by the intrinsic ER regeneration of the inversion process. At 2.5 Gb/s, a small penalty of 1.4 dB is suffered at a BER of 10^{-9} because the ER improvement is very small (ER_{in} = 5.9 dB, ER_{out} = 6.0 dB) and cannot correct for the signal degradation caused by the VCSEL itself. Overall however, the simultaneous demonstration of errorless performance with small power penalty, positive NM and ER regeneration proves that this inverter scheme can achieve cascadable operation at gigabit speed. This demonstration is the first of its kind using VCSEL technology at any wavelength.

5.3 Conclusion

As it has been shown, the proposed inverter scheme successfully achieves cascadable inverter operation up to 2.5 Gb/s using 1550 nm VCSELs based on the criterion of positive noise margins and ER regeneration. It is evident that faster, cascadable operation can be achieved when the VCSEL is biased further above threshold owing to the larger single pass gain. When compared with other competing

technologies such as semiconductor optical amplifiers (SOA) [7], the presented VCSEL inverter scheme offers an excellent tradeoff between switching power, speed, footprint and potential for large scale integration.

These results represent an important milestone towards the goal of an integrated OIP system at 1550 nm. It should be pointed out that these results were obtained with a commercially available VCSEL and that no device level optimization has been conducted for this study. In light of this fact, it is likely that significant improvements in the inverter characteristics can be made in terms of required power, speed and ER with future device design iterations. In support of this assertion, it is well known that the optimization of VCSOA device parameters such as top/bottom mirror reflectivity differ significantly from that of VCSELs [34]. It is conceivable that VCSEL specifications for logic applications contrast greatly with traditional VCSELs designed for low threshold lasing. Additionally, it is noted that 1550 nm VCSEL technology is still in an early stage of development. As it has been demonstrated in recent work [17], 850 nm VCSOAs, which are based on more mature technology, exhibit superior gain when compared to 1550 nm VCSOAs. It is believed that the inevitable device-level improvements of 1550 nm VCSELs will further advance the research area of VCSOA/VCSEL logic technology for applications in OIP in the telecommunications band.

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Optics Express, 2007 and "Low power optical bistability in 1550 nm VCSOAs," presented at CLEO, Baltimore, MD, 2007. The dissertation author and D. R. Jorgesen contributed equally to the first authorship of these publications.

Section 5.2 is, in part, a reprint of the material in "Cascadable optical inversion using a 1550 nm VCSEL" submitted to *Electronics Letters*, September 2007. The dissertation author was the primary investigator and first author.

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