1. Device Overview

1.1 General Description
NLTL-6273 is a MMIC non-linear transmission line (NLTL) based comb generator. This NLTL offers excellent phase noise performance over a low 0.7 to 5 GHz input frequency range with output tones beyond 40 GHz. NLTL-6273 is fabricated with GaAs Schottky diode based varactors on a 2.28 mm x 3.13 mm substrate. Both wire bondable die and connectorized modules are available.

1.2 Features
- Low Phase Noise
- Broadband Input Frequencies
- No External DC Bias Required

1.3 Applications
- Comb Line Generation
- High Efficiency Multiplication
- Samplers
- Phase Locked Loops

1.4 Functional Block Diagram

1.5 Part Ordering Options

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Package</th>
<th>Green Status</th>
<th>Product Lifecycle</th>
<th>Export Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>NLTL-6273CH</td>
<td>Wire bondable die</td>
<td>CH</td>
<td>RoHS</td>
<td>Active</td>
<td>EAR99</td>
</tr>
<tr>
<td>NLTL-6273S</td>
<td>Connectorized module, die wire bonded onto PCB</td>
<td>S</td>
<td></td>
<td>Active</td>
<td>EAR99</td>
</tr>
</tbody>
</table>

1 Refer to our website for a list of definitions for terminology presented in this table.
Table of Contents

1. Device Overview .................................. 1
   1.1 General Description .................. 1
   1.2 Features .................................. 1
   1.3 Applications ............................... 1
   1.4 Functional Block Diagram .......... 1
   1.5 Part Ordering Options ............... 1
2. Port Configurations and Functions ..... 3
   2.1 Port Diagram ............................... 3
   2.2 Port Functions ............................. 3
3. Specifications ................................. 4
   3.1 Absolute Maximum Ratings .......... 4
   3.2 Package Information ..................... 4
   3.3 Recommended Operating Conditions . 4
   3.4 Sequencing Requirements ............. 4
   3.5 Electrical Specifications .............. 5
   3.6 Typical Performance Plots .......... 6
      3.6.1 Typical Performance Plots:
         Residual Phase Noise ................. 10
4. Application Information ............... 11
   4.1 Detailed Description ................... 11
   4.2 Application Circuit ...................... 12
5. Die Mounting Recommendations ...... 13
   5.1 Mounting and Bonding
      Recommendations .......................... 13
   5.2 Handling Precautions ................... 13
   5.3 Bonding Diagram ......................... 14
6. Mechanical Data .............................. 15
   6.1 CH Package Outline Drawing ....... 15
   6.2 S Package Outline Drawing ............ 15

Revision History

<table>
<thead>
<tr>
<th>Revision Code</th>
<th>Revision Date</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>August 2017</td>
<td>Datasheet Initial Release</td>
</tr>
<tr>
<td>A</td>
<td>September 2017</td>
<td>Minor Clarification/Text Changes</td>
</tr>
<tr>
<td>B</td>
<td>October 2017</td>
<td>Corrected typos</td>
</tr>
<tr>
<td>C</td>
<td>August 2019</td>
<td>Added DC Current Plot</td>
</tr>
</tbody>
</table>
2. Port Configurations and Functions

2.1 Port Diagram
A top-down view of the NLTL-6273’s CH package outline drawing is shown below. The NLTL should only be used in the forward direction, with the input and output ports given in Port Functions.

![Port Diagram]

2.2 Port Functions

<table>
<thead>
<tr>
<th>Port</th>
<th>Function</th>
<th>Description</th>
<th>Equivalent Circuit for Chip</th>
<th>Equivalent Circuit for Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 1</td>
<td>Input</td>
<td>Port 1 is diode connected for the CH package and DC short for the S package.</td>
<td><img src="image" alt="P1" /></td>
<td><img src="image" alt="P1" /></td>
</tr>
<tr>
<td>Port 2</td>
<td>Output</td>
<td>Port 2 is diode connected for the CH and DC open for the S package.</td>
<td><img src="image" alt="P2" /></td>
<td><img src="image" alt="P2" /></td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>CH package ground path is provided through the substrate and ground bond pads. S package ground provided through metal housing and outer coax conductor.</td>
<td><img src="image" alt="GND" /></td>
<td><img src="image" alt="GND" /></td>
</tr>
</tbody>
</table>
3. Specifications

3.1 Absolute Maximum Ratings
The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 1 DC Current</td>
<td>TBD</td>
<td>mA</td>
</tr>
<tr>
<td>Port 2 DC Current</td>
<td>TBD</td>
<td>mA</td>
</tr>
<tr>
<td>Power Handling, at any Port</td>
<td>+TBD</td>
<td>dBm</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-55 to +100</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>

3.2 Package Information

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Details</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD</td>
<td>Human Body Model (HBM), per MIL-STD-750, Method 1020</td>
<td>TBD</td>
</tr>
<tr>
<td>Weight</td>
<td>S Package</td>
<td>10 g</td>
</tr>
</tbody>
</table>

3.3 Recommended Operating Conditions
The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Nominal</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_A$, Ambient Temperature</td>
<td>-55</td>
<td>+25</td>
<td>+100</td>
<td>°C</td>
</tr>
<tr>
<td>Input Power</td>
<td>+16</td>
<td></td>
<td>+26</td>
<td>dBm</td>
</tr>
</tbody>
</table>

3.4 Sequencing Requirements
This is a passive NLTL that requires no external DC bias. Self-bias of the diodes is sufficient for operation. It is not required, but is recommended to provide a 50Ω termination to each port before applying RF power.
3.5 Electrical Specifications

The electrical specifications apply at $T_A=+25^\circ$C in a 50Ω system. Typical data shown is for the NLTL used in the forward direction with a +20 dBm sine wave\(^2\) input.

Min and Max limits apply only to our connectorized units and are guaranteed at $T_A=+25^\circ$C. All bare die are 100% DC tested and visually inspected.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input (Port 1) Frequency Range</td>
<td>0.7</td>
<td>5</td>
<td></td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td>Output (Port 2) Frequency Range</td>
<td>0.7</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Power</td>
<td>+16</td>
<td>+26</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Maximum Output Harmonic for given Input</td>
<td>700 MHz Input</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>1 GHz Input</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>2 GHz Input</td>
<td>17</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>4 GHz Input</td>
<td>10</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>5 GHz Input</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^2\) Square Wave input generated using the ADM1-0026-5931SM and ADM1-0026-5929SM amplifier chain at +7 $V_d$ -0.5 $V_9$ with a +12 dBm input into the amplifier.
3.6 Typical Performance Plots

**Output Power vs Input Power: 0.7 GHz Sine Wave Input (dBm)**

- +16 dBm
- +18 dBm
- +20 dBm
- +22 dBm
- +24 dBm
- +26 dBm

Output Frequency (GHz)

This space intentionally left blank

**NTL Output for 0.7 GHz +24 dBm Sine Wave Input**

**Output Power vs Input Power: 1 GHz Sine Wave Input (dBm)**

Output Frequency (GHz)

This space intentionally left blank

**NTL Output for 0.7 GHz +24 dBm Sine Wave Input**

**NTL Output for 1 GHz +22 dBm Sine Wave Input**

**NTL Output for 1 GHz +22 dBm Sine Wave Input**
This space intentionally left blank
Output Power vs Input Power: 5 GHz Sine Wave Input (dBm)

- +16 dBm (▲)
- +18 dBm (▲)
- +20 dBm (▲)
- +22 dBm (▲)
- +24 dBm (▲)
- +26 dBm (▲)

Output Frequency (GHz)

This space intentionally left blank

DC Rectified Current vs. Input Power, 1 GHz Input (mA)

Input Power (dBm)

15 17 19 21 23 25 27

0 50 100 150 200

5 GHz +24 dBm Sine Wave Input

NLTL Output for 5 GHz +24 dBm Sine Wave Input
3.6.1 Typical Performance Plots: Residual Phase Noise

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Min</th>
<th>Typical</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Hz Offset</td>
<td>-120</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>10 Hz Offset</td>
<td>-130</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>100 Hz Offset</td>
<td>-140</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>1 KHz Offset</td>
<td>-150</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>10 KHz Offset</td>
<td>-160</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>100 KHz Offset</td>
<td>-170</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
<tr>
<td>1 MHz Offset</td>
<td>Thermal Floor</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
</tbody>
</table>
4. Application Information

4.1 Detailed Description
NLTL-6273 belongs to Marki Microwave’s NLTL family of multipliers and non-linear transmission lines. The NLTL product line consists of passive GaAs MMIC non-linear transmission lines designed and fabricated with GaAs Schottky diode based varactors. NLTLs take an input signal and create an impulse train of harmonics. Harmonic outputs up to and beyond 40 GHz are generated by the NLTL. The NLTL-6273SM is the packaged 5 mm QFN version of the NLTL-6273CH.

Port 1 supports L and S band input signals. Port 2 will output integer multiples of the input signal (i.e., x2, x3, x4, …, x30) up to the 30th output harmonic or a maximum of 40 GHz. Higher harmonics can be generated but will be at a lower efficiency.

The operating conditions of the NLTL are extremely important to optimize performance. High power inputs will increase the output power observed; however, the conversion efficiency will decrease. This is increasingly true for higher input frequencies and at input powers above the recommended limit. Optimal conversion efficiency of the NLTL is achieved using a square wave input with a fast rise time. Doing so causes a degradation in the 2nd output harmonic but otherwise improves the conversion efficiency at all other harmonics.

NLTL-6273 requires no external DC bias. The self-bias of the diodes caused by the rectified RF input signal is sufficient for operation. For the best performance, optimization of the DC return path is recommended for each specific application to optimize the harmonic output power distribution.

The phase noise of a non-linear transmission line is outstanding. If verification of performance is necessary, the application circuit used and input conditions are extremely important. NLTLs are AM sensitive. If there is excessive AM noise on the input of the NLTL, observing the output of the NLTL will show excessive PM/phase noise because of the high AM to PM conversion property of NLTLs.
4.2 Application Circuit

**DC Path to Ground** — An RF choke followed by a 15 Ω resistor should be used to provide a DC path to ground on the input port of the NLTL. A shunt 1 μF capacitor is used to filter noise generated by the resistor. This forms the circuit which self-biases the NLTL. The DC return to ground removes DC rectified current created by high power RF signal injection. The DC path to ground is provided within the S package. A conical coil inductor is recommended to push the self-resonance frequency of the inductor past the operating bandwidth of the NLTL. The recommended inductance value of the conical coil inductor is 50nH or higher.

**Blocking Capacitor** — A DC blocking capacitor on the output of the NLTL-6273’s integrated circuit is necessary to prevent unwanted DC current flow from or to the output. If there is a DC signal on the input, place a DC block on the input to avoid disrupting the self-biasing of the diodes.
5. Die Mounting Recommendations

5.1 Mounting and Bonding Recommendations
Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

**Mounting** - To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy according to manufacturer instructions.

**Wire Bonding** - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).

**Circuit Considerations** – 50 Ω transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001” thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

5.2 Handling Precautions

**General Handling**
Chips should be handled with care using tweezers or a vacuum collet. Users should take precautions to protect chips from direct human contact that can deposit contaminants, like perspiration and skin oils on any of the chip's surfaces.

**Static Sensitivity**
GaAs MMIC devices are sensitive to ESD and should be handled, assembled, tested, and transported only in static protected environments.

**Cleaning and Storage**: Do not attempt to clean the chip with a liquid cleaning system or expose the bare chips to liquid. Once the ESD sensitive bags the chips are stored in are opened, chips should be stored in a dry nitrogen atmosphere.
5.3 Bonding Diagram

- **Output**
- **Orientation Marker**
- **Substrate connected to ground with conductive epoxy**
- **Multiple Wirebonds for Reduced Inductance**
- **Input**
- **Minimum Space Gap/Wirebond Length**
6. Mechanical Data

6.1 CH Package Outline Drawing

1. CH Substrate material is 0.004 in thick GaAs.
2. I/O trace finish is 4.2 microns Au. Ground plane finish is 5 microns Au.
3. XXXX denotes circuit number.

6.2 S Package Outline Drawing

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