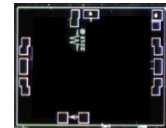
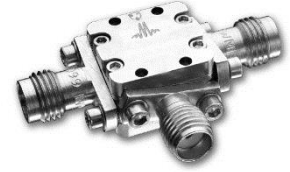


# GaAs MMIC Double Balanced Mixer

# MM1-0626H

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The MM1-0626H is a passive double balanced MMIC mixer. It features excellent conversion loss, superior isolations and spurious performance across a broad bandwidth, in a highly miniaturized form factor. Accurate, nonlinear simulation models are available for Microwave Office® through the Marki Microwave PDK. The MM1-0626H is available as a wire bondable chip or an SMA connectorized package. The MM1-0626H is a superior alternative to Marki Microwave carrier and packaged M1 and M3 mixers.



## Features

- Compact Chip Style Package (0.054" x 0.046"x0.004")
- CAD Optimized for Superior Isolation and Spurious Response
- Broadband Performance
- Excellent Unit-to-Unit Repeatability
- Fully nonlinear software models available with Marki PDK for Microwave Office®
- RoHS Compliant

**Electrical Specifications** - Specifications guaranteed from -55 to +100°C, measured in a 50Ω system. Specifications are shown for Configurations A (B). See page 2 for port locations. All bare die are 100% DC tested and 100% visually inspected. RF testing is performed on a sample basis to verify conformance to datasheet guaranteed specifications. Consult factory for more information.

Parameter	LO (GHz)	RF (GHz)	IF (GHz)	Min	Typ	Max	LO drive level (dBm)
Conversion Loss (dB)	6-26.5	6-26.5	DC-9		7.5 (9)		+15 (+15)
Isolation (dB)							
LO-RF				47			
LO-IF				34			
RF-IF				35			Config. A: + 13 to + 20 Config. B: + 13 to + 20
Input 1 dB Compression (dBm)				+9 (+9)			
Input Two-Tone Third Order Intercept Point (dBm) <sup>2</sup>				+21 (+23)			

## Part Number Options

<i>Please specify diode level and package style by adding to model number.</i>				
Package Styles		Examples		
Connectorized <sup>1, 3</sup>	S	MM1-0626HCH-2, MM1-0626HS		
Chip <sup>2, 3</sup> (RoHS)	CH-2	<u>MM1-0626</u> (Model)	<u>H</u> (Diode Option)	<u>S</u> (Package)

<sup>1</sup>Connectorized package consists of chip package wire bonded to a substrate, equivalent to an evaluation board.

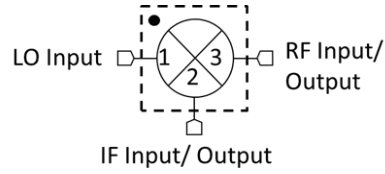
<sup>2</sup>Chip package connects to external circuit through wire bondable gold pads.

<sup>3</sup>Note: For port locations and I/O designations, refer to the drawings on page 2 of this document.

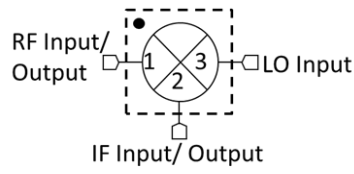
# GaAs MMIC Double Balanced Mixer

# MM1-0626H

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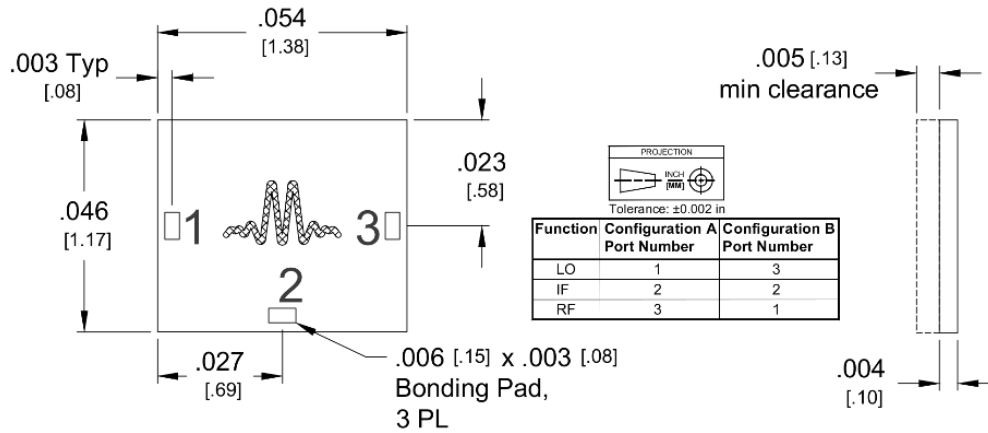


**Configuration A**

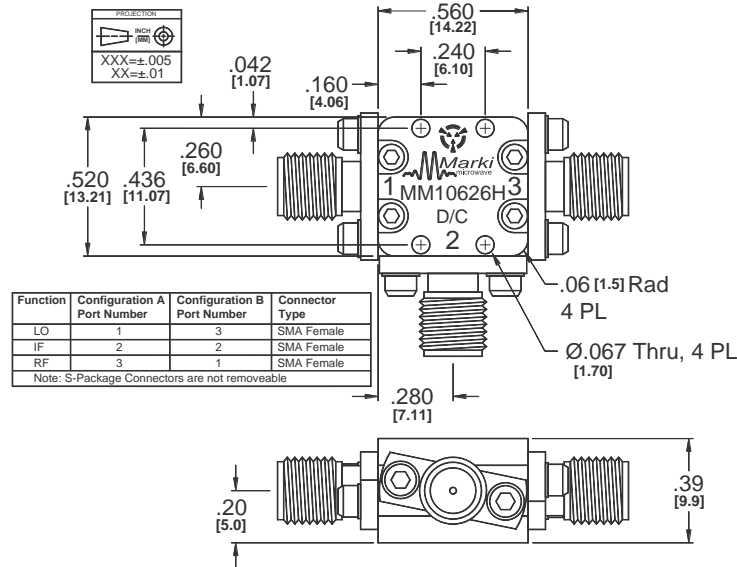


**Configuration B**

1. Configuration A/B refer to the same part number (MM1-0626H) used in one of two different ways for optimal spurious performance. For the lowest conversion loss, use the mixer in Configuration A (port 1 as the LO input, port 2 as the RF input or output). If you need to use a lower LO drive, use the mixer in Configuration B (port 1 as the RF input or output, port 2 as the LO input). For optimal spurious suppression, experimentation or simulation is required to choose between Configuration A and B. For more information, [see here](#).



1. CH Substrate material is .004 in thick GaAs.
2. I/O traces finish is 4.2 microns Au. Ground plane finish is 5 microns Au.
3. Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).

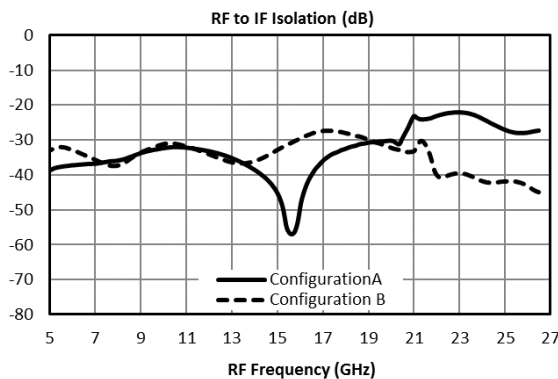
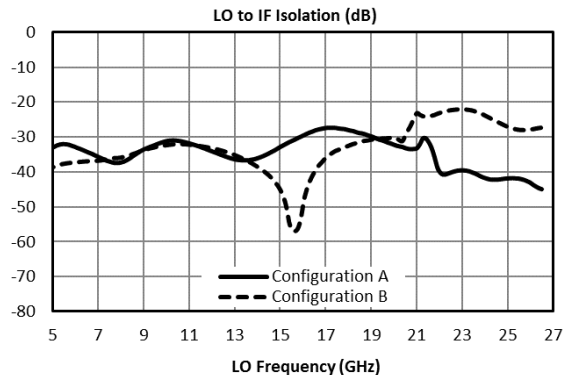
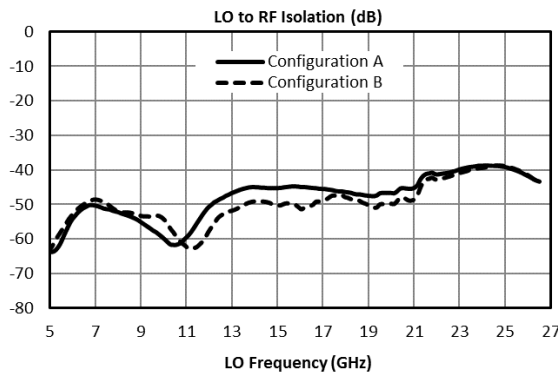
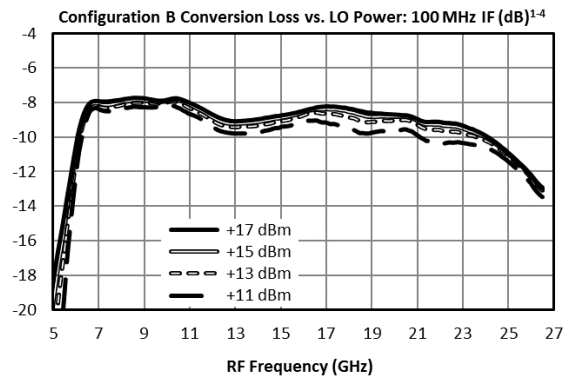
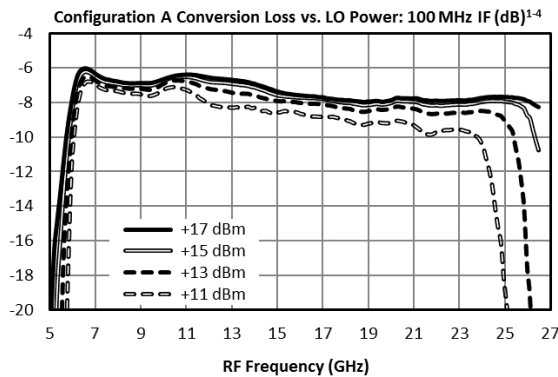
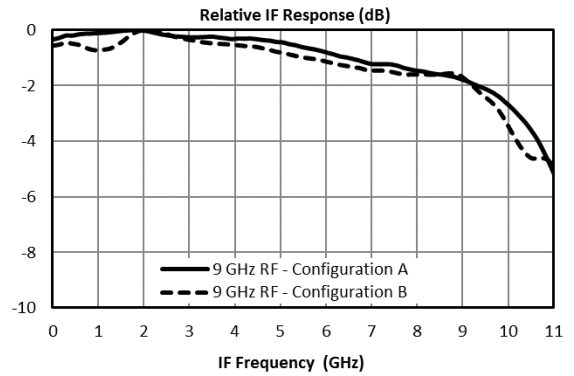
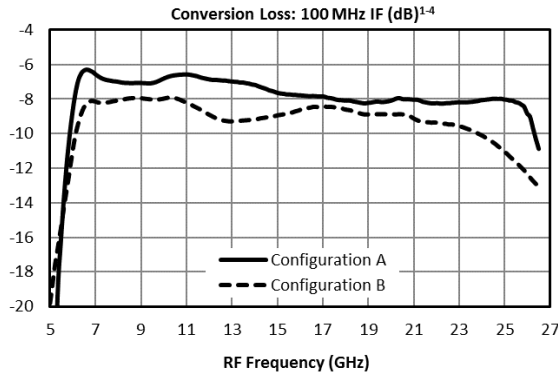


# GaAs MMIC Double Balanced Mixer

# MM1-0626H

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## Typical Performance

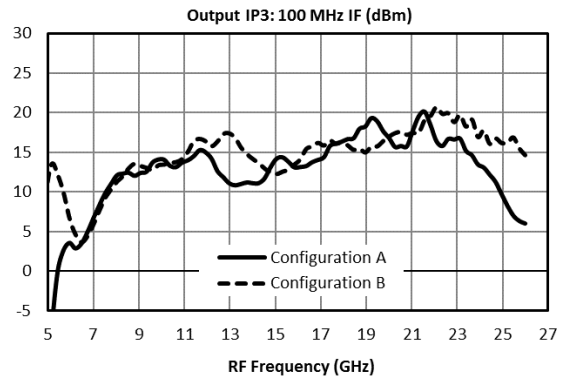
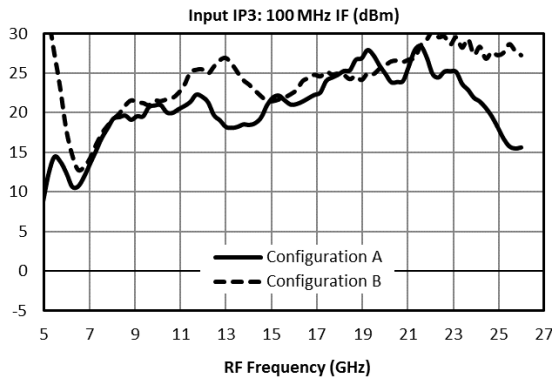
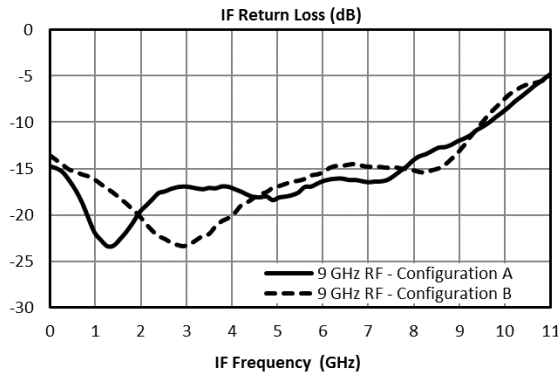
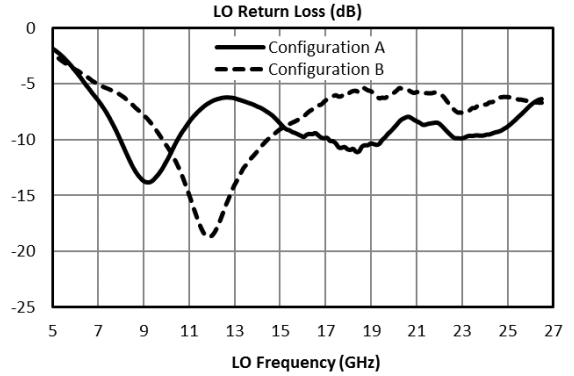
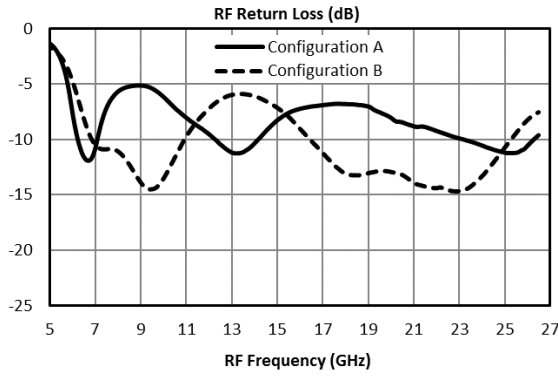


# GaAs MMIC Double Balanced Mixer

# MM1-0626H

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## Typical Performance

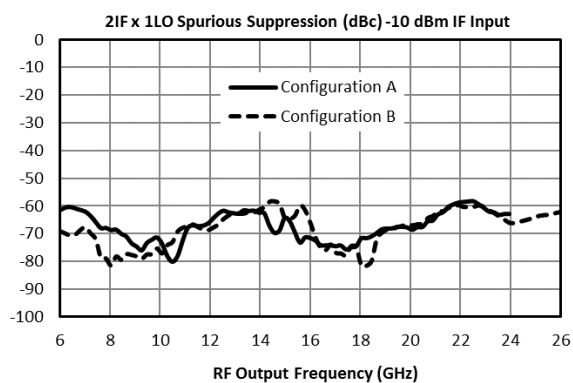
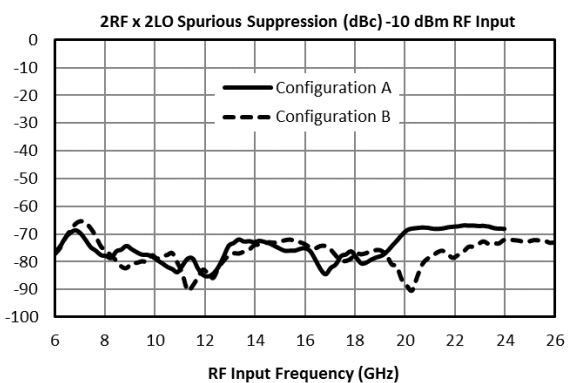
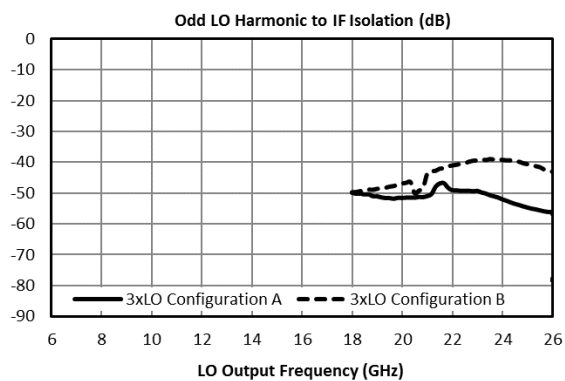
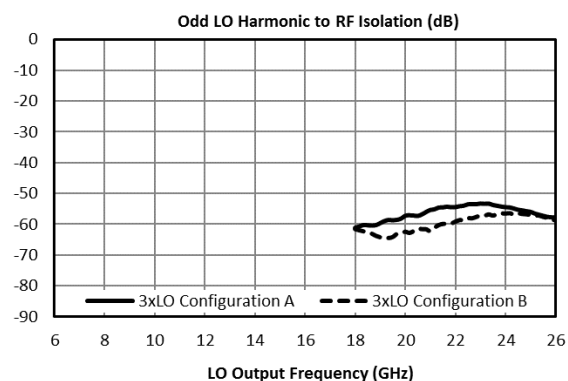
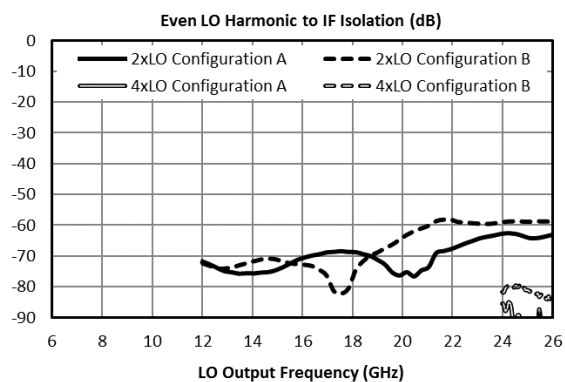
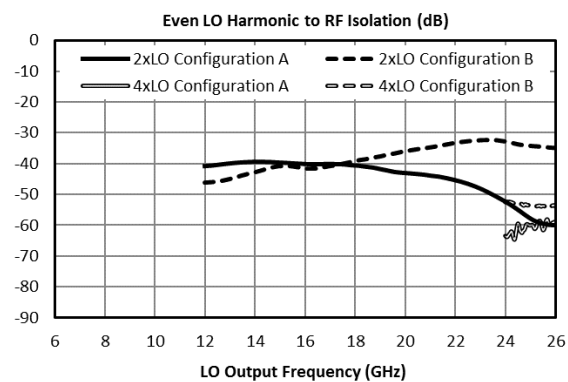


# GaAs MMIC Double Balanced Mixer

# MM1-0626H

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## Typical Performance



**Downconversion Spurious Suppression**

Spurious data is taken by selecting RF and LO frequencies ( $\pm mLO \pm nRF$ ) within the 6 to 26 GHz RF/LO bands, which create a 91 MHz IF spurious output. The mixer is swept across the full spurious band and the mean is calculated. The numbers shown in the table below are for a -10 dBm RF input. Spurious suppression is scaled for different RF power levels by (n-1), where “n” is the RF spur order. For example, the 2RFx2LO spur is 75 dBc for the A configuration for a -10 dBm input, so a -20 dBm RF input creates a spur that is (2-1) x (-10 dB) dB lower, or 85 dBc.

**Typical Downconversion Spurious Suppression (dBc): A Configuration (B Configuration), Sine Wave LO <sup>5</sup>**

<b>-10 dBm RF Input</b>	0xLO	1xLO	2xLO	3xLO	4xLO	5xLO
1xRF	25 (26)	Reference	31 (45)	13 (12)	34 (47)	15 (18)
2xRF	76 (77)	70 (54)	75 (77)	68 (58)	74 (78)	69 (67)
3xRF	112 (112)	62 (64)	86 (95)	72 (81)	82 (96)	68 (73)
4xRF	136 (139)	116 (100)	117 (118)	118 (108)	115 (119)	116 (107)
5xRF	N/A	114 (134)	126 (134)	117 (125)	128 (132)	115 (126)

**Upconversion Spurious Suppression**

Spurious data is taken by mixing a 91 MHz IF with LO frequencies ( $\pm mLO \pm nIF$ ), which creates an RF within the 6 to 26 GHz RF band. The mixer is swept across the full spurious output band and the mean is calculated. The numbers shown in the table below are for a -10 dBm IF input. Spurious suppression is scaled for different IF input power levels by (n-1), where “n” is the IF spur order. For example, the 2IFx1LO spur is typically 67 dBc for the A configuration for a -10 dBm input, so a -20 dBm IF input creates a spur that is (2-1) x (-10 dB) dB lower, or 77 dBc.

**Typical Upconversion Spurious Suppression (dBc): A Configuration (B Configuration), Sine Wave LO <sup>5</sup>**

<b>-10 dBm RF Input</b>	0xLO	1xLO	2xLO	3xLO	4xLO	5xLO
1xIF	29 (24)	Reference	32 (47)	10 (10)	31 (55)	22 (25)
2xIF	71 (59)	67 (68)	66 (56)	68 (72)	62 (59)	68 (67)
3xIF	111 (112)	69 (70)	78 (91)	60 (64)	78 (92)	66 (68)
4xIF	125 (103)	117 (116)	108 (100)	114 (118)	105 (103)	113 (115)
5xIF	130 (144)	113 (116)	122 (130)	112 (119)	120 (133)	110 (111)

**Mounting and Bonding Recommendations**

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

**Mounting** - To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy according to manufacturer instructions.

**Wire Bonding** - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).

**Circuit Considerations** – 50 Ω transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001” thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

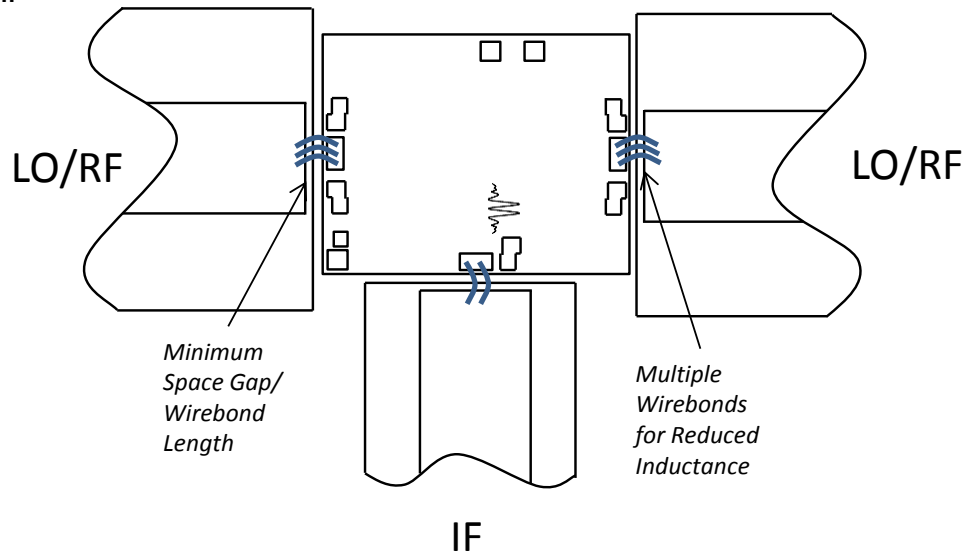
**Handling Precautions**

**General Handling:** Chips should be handled with care using tweezers or a vacuum collet. Users should take precautions to protect chips from direct human contact that can deposit contaminants, like perspiration and skin oils on any of the chip’s surfaces.

**Static Sensitivity:** GaAs MMIC devices are subject to static discharge, and should be handled, assembled, tested, and transported only in static protected environments.

**Cleaning and Storage:** Do not attempt to clean the chip with a liquid cleaning system or expose the bare chips to liquid. Once the ESD sensitive bags the chips are stored in are opened, chips should be stored in a dry nitrogen atmosphere.

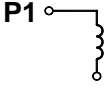
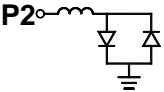
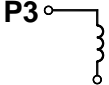
**Bonding Diagram**



# GaAs MMIC Double Balanced Mixer

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Port	Description	DC Interface Schematic
Port 1	Port 1 is DC open and AC matched to 50 Ohms from 6 to 26.5 GHz. Blocking capacitor is optional.	
Port 2	Port 2 is DC coupled to the diodes. Blocking capacitor is optional.	
Port 3	Port 3 is DC open and AC matched to 50 Ohms from 6 to 26.5 GHz. Blocking capacitor is optional.	

Absolute Maximum Ratings	
Parameter	Maximum Rating
Port 1 DC Current	N/A
Port 2 DC Current	15 mA
Port 3 DC Current	N/A
RF Power Handling (RF+LO)	+32 dBm at +25°C, derated linearly to +20 dBm at +100°C
Operating Temperature	-55°C to +100°C
Storage Temperature	-65°C to +125°C

**DATA SHEET NOTES:**

1. Mixer Conversion Loss Plot IF frequency is 100 MHz.
2. Mixer Noise Figure typically measures within 0.5 dB of conversion loss for IF frequencies greater than 5 MHz.
3. Conversion Loss typically degrades less than 0.5 dB at +100°C and improves less than 0.5 dB at -55°C.
4. Unless otherwise specified, data is taken with +15 dBm lowside LO drive.
5. Specifications are subject to change without notice. Contact Marki Microwave for the most recent specifications and data sheets.
6. Catalog mixer circuits are continually improved. Configuration control requires custom mixer model numbers and specifications.

Note: Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.





## GaAs MMIC Double Balanced Mixer

**MM1-0626H**

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### Revision History

Revision Code	Revision Date	Comment
A	November 2017	Die shrunk from 1.48 x 1.18 mm <sup>2</sup> to 1.37 x 1.17 mm <sup>2</sup> . CH package tolerance added.

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