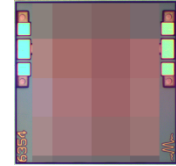


1 Device Overview

1.1 General Description

The MFB-2500 is a passive MMIC bandpass filter. It is a low loss integrated filter that passes K-Band and lower Ka-Band frequencies (18-32GHz). Passive GaAs MMIC technology allows production of smaller filter constructions that replace larger form factor circuit board constructions. Tight fabrication tolerances allow for less unit to unit variation than traditional filter technologies. The MFB-2500 is available as a wire bondable chip. Low unit to unit variation allow for accurate simulations using the provided S2P file taken from measured production units.



Bare Die

1.2 Features

- Designed for K-Band, Ka-Band, 5G, and SATCOM Applications
- Insertion Loss Typically 1.5dB at Center Frequency
- Excellent Return Loss
- High Stop Band Suppression
- Wide Stop Band
- S2P data: [MFB-2500.zip](#)

1.3 Functional Block Diagram



1.4 Part Ordering Options¹

| Part Number | Description | Package | Green Status | Product Lifecycle | Export Classification |
|-------------|-------------------|---------|--------------|-------------------|-----------------------|
| MFB-2500CH | Wire bondable die | CH | RoHS | Active | EAR99 |

¹ Refer to our [website](#) for a list of definitions for terminology presented in this table.

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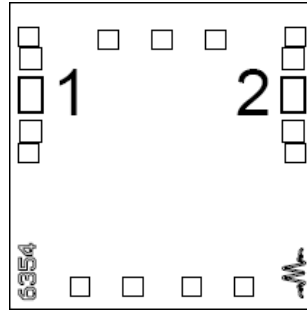
Revision History

| Revision Code | Revision Date | Comment |
|---------------|---------------|---------------------------|
| - | January 2018 | Datasheet Initial Release |

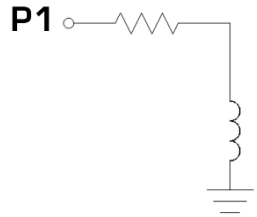
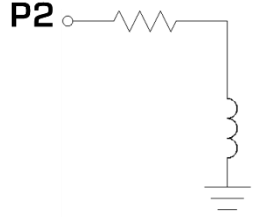
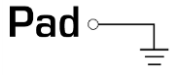
2 Port Configurations and Functions

2.1 Port Diagram

A top-down view of the MFB-2500CH package outline drawing is shown below. The MMIC bandpass filters are symmetrical allowing Port 1 or Port 2 to be used as the input.



2.2 Port Functions

| Port | Function | Description | Equivalent Circuit |
|--------|--------------|---|---|
| Port 1 | Input/Output | Port 1 is DC connected to ground through a resistor. DC block is required if voltage present. |  |
| Port 2 | Input/Output | Port 2 is DC connected to ground through a resistor. DC block is required if voltage present. |  |
| Pad | Ground | CH package ground path is provided through the substrate and ground bond pads. |  |

3 Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

| Parameter | Maximum Rating | Units |
|-----------------------------|----------------|-------|
| Port 1 DC Current | 40 | mA |
| Port 2 DC Current | 40 | mA |
| Power Handling, at any Port | +30 | dBm |
| Operating Temperature | -55 to +100 | °C |
| Storage Temperature | -65 to +125 | °C |

3.2 Package Information

| Parameter | Details | Rating |
|-----------|--|--------|
| ESD | Human Body Model (HBM), per MIL-STD-750, Method 1020 | TBD |

3.3 Electrical Specifications²

The electrical specifications apply at $T_A=+25^\circ\text{C}$ in a 50Ω system.

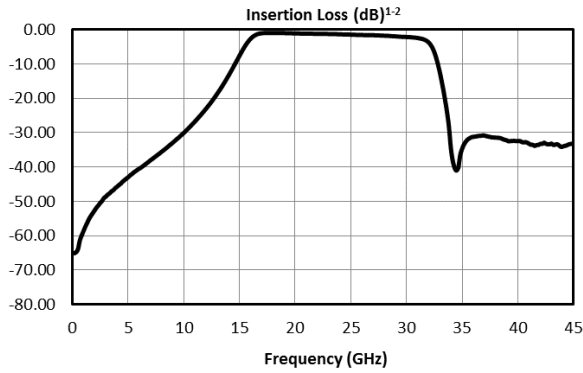
Min and Max limits are guaranteed at $T_A=+25^\circ\text{C}$. All bare die are 100% DC tested and visually inspected.

| Parameter | Frequency (GHz) | Min | Typ. | Max |
|-------------------------------|-------------------|----------|----------|-----|
| Center Frequency, f_c (GHz) | | | 25 | |
| Passband (GHz) | | | 18-32 | |
| Insertion Loss @ f_c (dB) | | | 1.5 | 3 |
| Passband Return Loss (dB) | 18-32 | | 15 | |
| Stopband Suppression (dB) | 2.5 10.0, 34.0 | 40 25 | 50 30 | |
| Impedance (Ω) | | | 50 | |

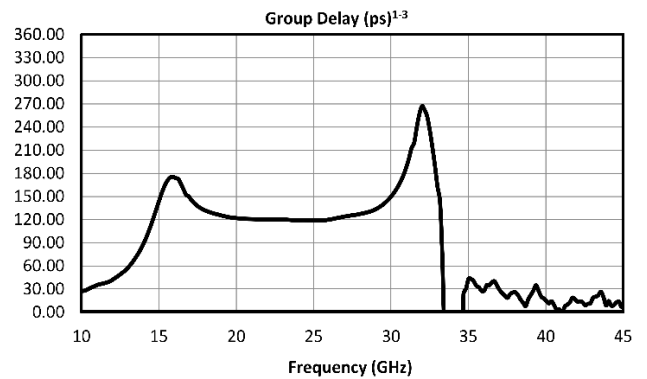
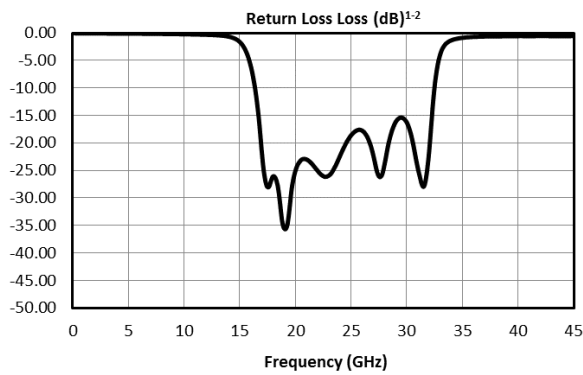
² Equalizer is symmetrical. Reverse measurement is equivalent to forward measurement.

3.4 Typical Performance Plots

3.4.1 Insertion Loss



3.4.2 Return Loss & Group Delay³



¹ Filter is symmetrical. Reverse measurement is equivalent to forward measurement.

² All measured data is taken and simulations assume 50 Ω probes on chip.

³ Group delay calculated using wrapped phase response.

4 Die Mounting Recommendations

4.1 Mounting and Bonding Recommendations

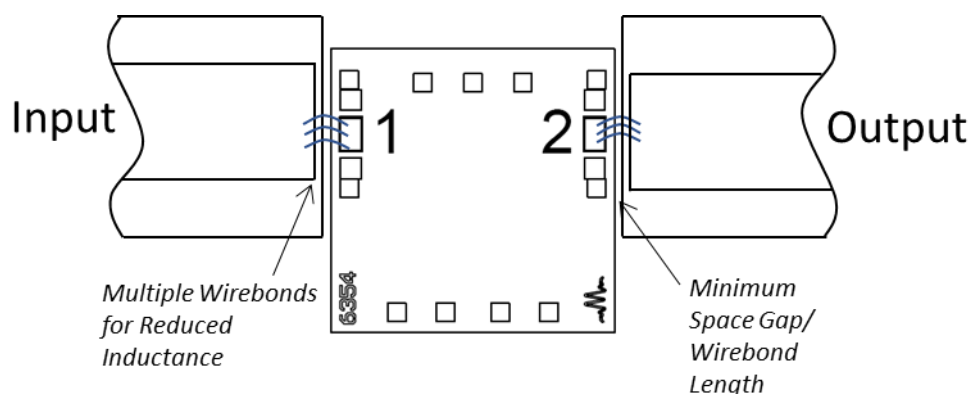
Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy according to manufacturer instructions.

Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).

Circuit Considerations – 50 Ω transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001" thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

4.2 Bonding Diagram



4.3 Handling Precautions

General Handling

Chips should be handled with care using tweezers or a vacuum collet. Users should take precautions to protect chips from direct human contact that can deposit contaminants, like perspiration and skin oils on any of the chip's surfaces.

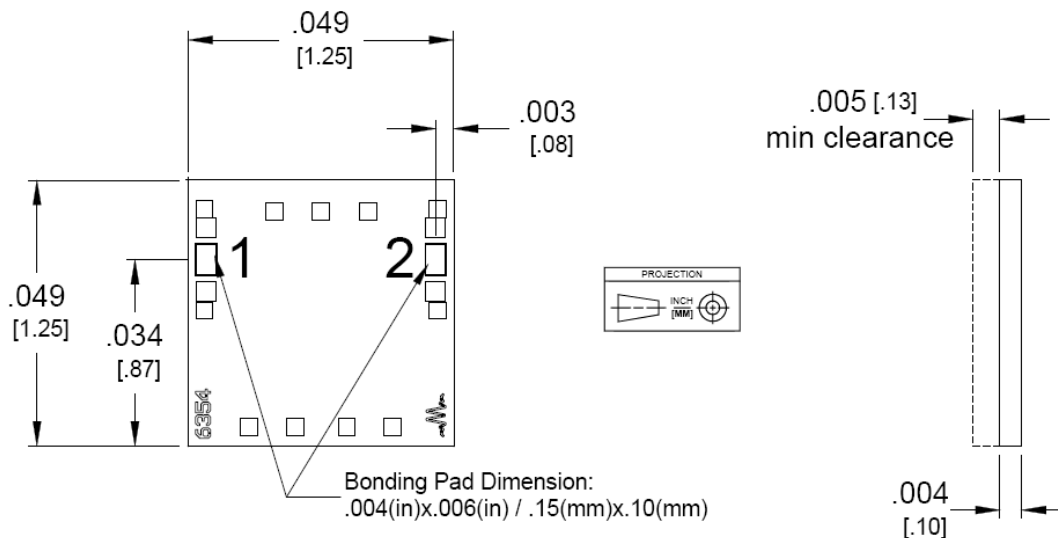
Static Sensitivity

GaAs MMIC devices are sensitive to ESD and should be handled, assembled, tested, and transported only in static protected environments.

Cleaning and Storage: Do not attempt to clean the chip with a liquid cleaning system or expose the bare chips to liquid. Once the ESD sensitive bags the chips are stored in are opened, chips should be stored in a dry nitrogen atmosphere.

5 Mechanical Data

5.1 CH Package Outline Drawing



1. CH Substrate material is 0.004 in thick GaAs.
2. I/O trace finish is 5 microns Au. Ground plane finish is 4 microns Au.

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