MEQ Device Overview

1.1 General Description
The MEQ10-45CSP1 is a passive MMIC equalizer QFN ideal for compensating for low pass filtering effects in RF/microwave and high speed digital systems. The MEQ10-45CSP1 provides positive slope from DC to 45GHz with a DC attenuation of 10dB. The new chip scale package allows for extreme miniaturization of the SMT footprint. The unique design offers superior return loss to competitors in an extremely small footprint. GaAs MMIC technology provides consistent unit-to-unit performance in a small, low cost form factor.

1.2 Features
- Small 1.5 x 1.5 mm package size
- DC attenuation of 10dB
- Typical Insertion Loss 0.7 dB at 45GHz
- Typical VSWR of 1.5 Over Operating Band
- Low SWaP
- S2P data: MEQ10-45CSP1.s2p

1.3 Applications
- RF Transceivers
- High-Speed Data
- Telecom
- Cable Loss Compensation
- Amplifier Compensation

1.4 Functional Block Diagram

1.5 Part Ordering Options

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Loss at DC (dB)</th>
<th>Description</th>
<th>Package</th>
<th>Green Status</th>
<th>Product Lifecycle</th>
<th>Export Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEQ10-45CSP1</td>
<td>10</td>
<td>1.5 x 1.5 mm QFN</td>
<td>CSP1</td>
<td>RoHS</td>
<td>Active</td>
<td>EAR99</td>
</tr>
<tr>
<td>EVB-MEQ10-45</td>
<td>10</td>
<td>Connectorized Evaluation Module</td>
<td>Module</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Refer to our [website](#) for a list of definitions for terminology presented in this table.
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Revision History

<table>
<thead>
<tr>
<th>Revision Code</th>
<th>Revision Date</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>March 2022</td>
<td>Datasheet Initial Release</td>
</tr>
<tr>
<td>A</td>
<td>June 2022</td>
<td>Outline Drawing and evaluation board name updated</td>
</tr>
</tbody>
</table>
# Port Configurations and Functions

## 2.1 Port Diagram
An x-ray view of the MEQ10-45CSP1 package outline drawing is shown below. The MEQ equalizers are symmetrical allowing Port 1 or Port 2 to be used as the input.

![Port Diagram](image)

## 2.2 Port Functions

<table>
<thead>
<tr>
<th>Port</th>
<th>Function</th>
<th>Description</th>
<th>Equivalent Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1</td>
<td>Input/Output</td>
<td>Pin 1 is DC connected to ground through a resistor. DC block is required if voltage present.</td>
<td><img src="image" alt="P1" /></td>
</tr>
<tr>
<td>Pin 2</td>
<td>Input/Output</td>
<td>Pin 2 is DC connected to ground through a resistor. DC block is required if voltage present.</td>
<td><img src="image" alt="P2" /></td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>SM package ground path is provided through the ground paddle.</td>
<td><img src="image" alt="Pad" /></td>
</tr>
</tbody>
</table>
3 Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature</td>
<td>-55 to +100</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>

3.2 Package Information

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Details</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD</td>
<td>Human Body Model (HBM), per MIL-STD-750, Method 1020</td>
<td>TBD</td>
</tr>
</tbody>
</table>

3.3 Electrical Specifications

The electrical specifications apply at $T_A=+25^\circ C$ in a $50\Omega$ system. Typical data shown is for the equalizer in a SM package with a sine wave input applied to port 1.

Min and Max limits are guaranteed at $T_A=+25^\circ C$. All bare die are 100% DC tested and visually inspected.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Frequency Range (GHz)</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insertion Loss (dB)</td>
<td>DC</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>45</td>
<td>0.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Return Loss (dB)</td>
<td>DC to 45</td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Impedance (Ω)</td>
<td>DC to 45</td>
<td>50</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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2 Equalizer is symmetrical. Reverse measurement is equivalent to forward measurement. All measurements taken in EVB package and de-embedded to the CSP1 pad interface.
3.4 Typical Performance Plots

3.4.1 Electrical Performance

*Electrical Performance Plots are de-embedded to the CSP package ports*

3.4.2 Electrical Performance Over Temperature

*Evaluation board performance is shown as a proxy for device performance due to fixturing variability over temperature*
4 Mechanical Data

4.1 CSP1 Package Outline Drawing

Unless otherwise specified, dimensions are in inches. Tolerances are:

- .X ± 0.1
- .XXX ± 0.004

1. Front to back registration to be 50.8µm max.
2. Circuits to be shipped individually.
3. Shaded areas are metalized.
4. Finish: Ni: 0.5 - 2.5 µm
   Pd: 0.02 - 0.15 µm
   Au: 0.003 - 0.015 µm

4.2 CSP1 Package Footprint

- Recommended to have the ground plane flooded. Ground plane are left to PCB designer's discretion.

Ø.010 Plated thru via epoxy filled. Recommended conductive or non-conductive fill, 6 PL. Vias can be added or reduced at PCB designer's discretion.

The landing pattern is to be used on Rogers4003, 0.008" thick, ½ Oz Cu.

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Click here for a DXF of the above layout.
Click here for leaded solder reflow. Click here for lead-free solder reflow
4.3 EVB Package Outline Drawing

Unless otherwise specified, dimensions are in inches. Tolerances are:

\[
\begin{align*}
XX & \pm 0.02 \\
XXX & \pm 0.005 \\
\end{align*}
\]