

LEAD-FREE / RoHS-COMPLIANT

SURFACE-MOUNT BROADBAND BALUN

BAL-0020SLG

Features

- 10 MHz to 20 GHz 1:2 Balun (Balanced to Unbalanced Transformer)
- Transforms 50 Ω Input to 100 Ω Differential (50 Ohm Single) Output
- Tuned for Optimal Phase/Amplitude Balance
- Applications: Analog to Digital Converters, Balanced Receivers, Baseband Digital Modulation, Signal Integrity
- [BAL-0020SLG.s3p](#)



SMT

Electrical Specifications - Specifications guaranteed from -55 to +100°C, measured in a 50 Ω system.

Parameter	Frequency Range	Min	Typ	Max
Insertion Loss as a mode converter (dB)	10 MHz to 20 GHz		4.5	7
Nominal Phase Shift (Degrees)			180	
Amplitude Balance (dB)			0.4	1.2
Phase Balance (Degrees)			5	10
Common Mode Rejection (dB)		22	35	
Isolation (dB)			12	
VSWR (Common)			1.5	
VSWR (Output)			1.6	
Total Input Power (W)				

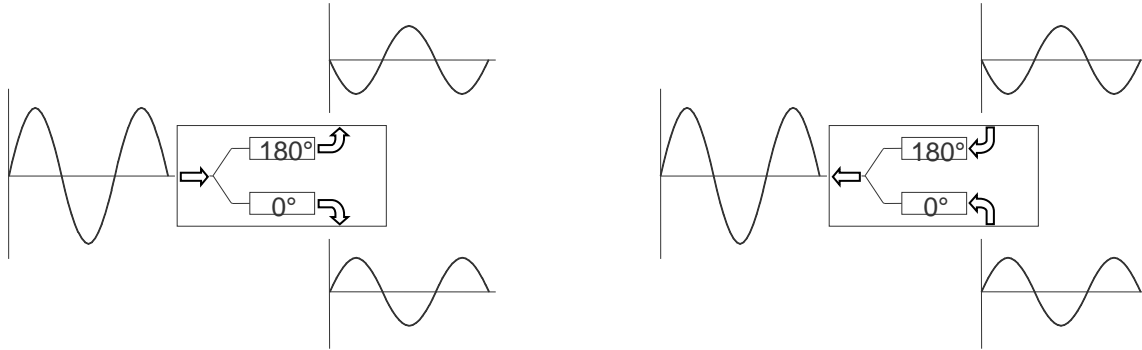
Model Number	Description
BAL-0020SLG	10 MHz to 20 GHz Balun, Surface Mount, LEAD-FREE/RoHS COMPLIANT
EVAL-BAL-0020	Connectorized Evaluation Fixture, LEAD-FREE/RoHS COMPLIANT

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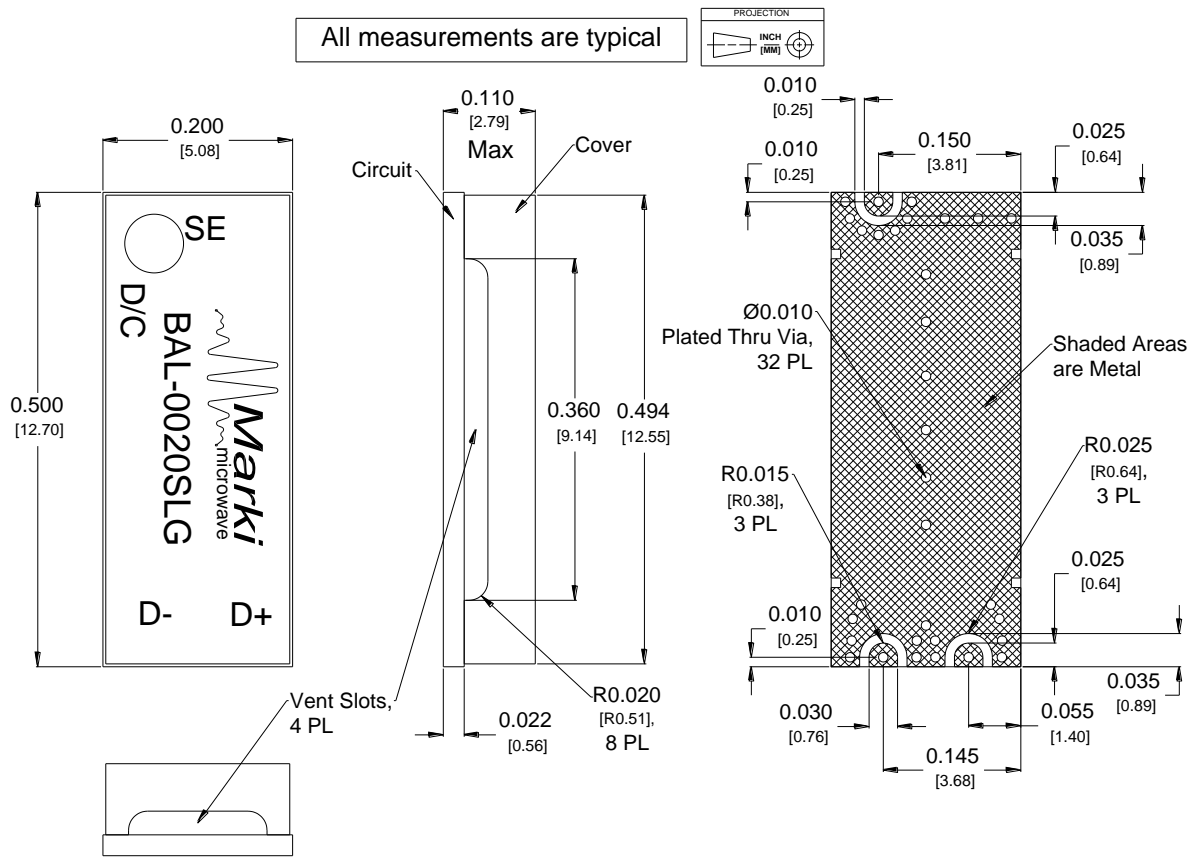
Block Diagram



Single ended to differential

Differential to single ended

Outline Drawing



Material is FR4 ,Finish is 2-8μ-inches of Gold type III Grade A, Soft Gold over 100-200 μ-inches solderable Nickel.

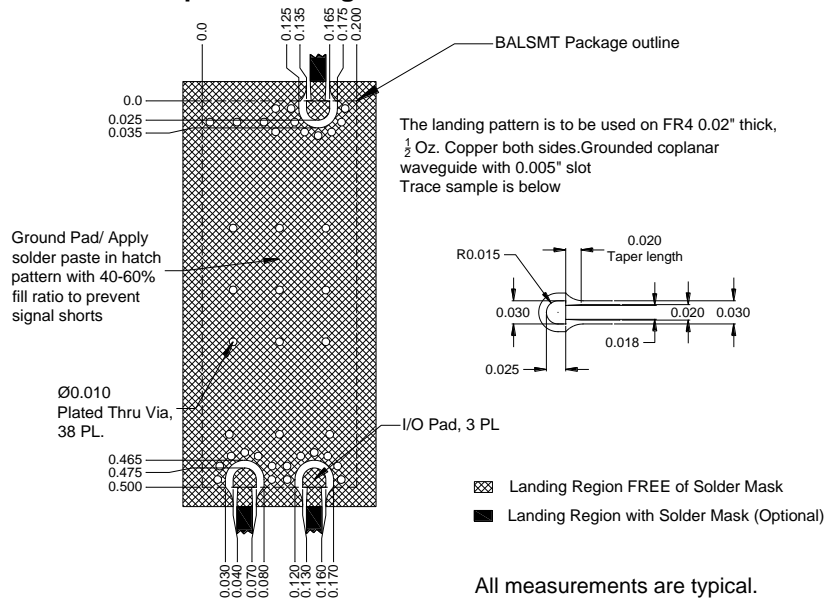
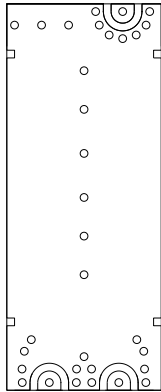
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PCB Footprint Drawing

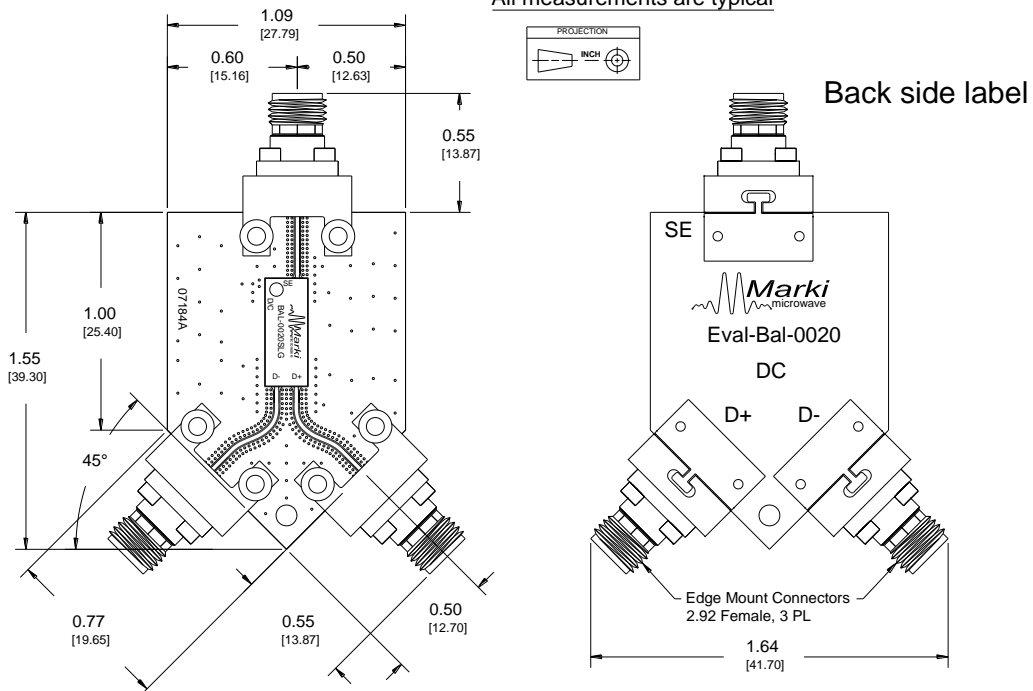
Balun SMT Package
See Through View



[Click here for a DXF of the above layout.](#)

Eval Package Outline Drawing

All measurements are typical



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Mixed Mode Scattering Parameters¹

Mixed mode scattering parameters are used to characterize differential circuits. For baluns, this means that the 0° and 180° ports become a single 100Ω differential port and the common port remains the same 50Ω common port. The two-port s-parameters of the balun are then characterized based on differential (d), common mode (c), or single-ended (s) signals. For example: Sds21 is the differential output response given a single ended input.

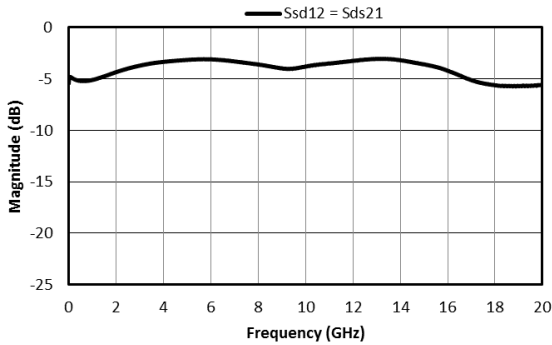


Fig. 1. Insertion loss as a mode converter

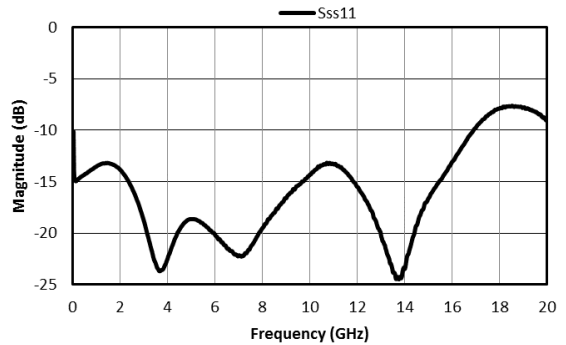


Fig. 2. Unbalanced port return loss

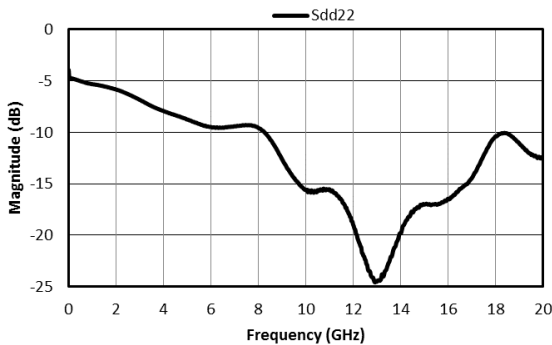


Fig. 3. Differential port return loss

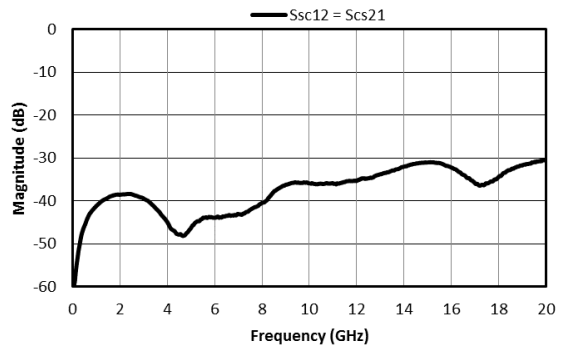


Fig. 4. Insertion loss of a common mode signal

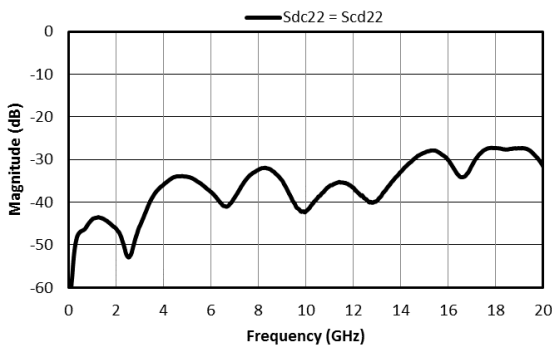


Fig. 5. Reflection converted between differential and common modes

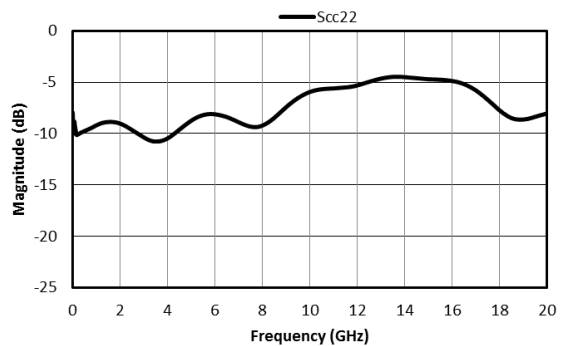


Fig. 6. Return loss of a common mode signal

Typical Performance Scattering Parameter

Three port scattering parameters measured as three single-ended 50Ω ports showing relationship between any two ports.

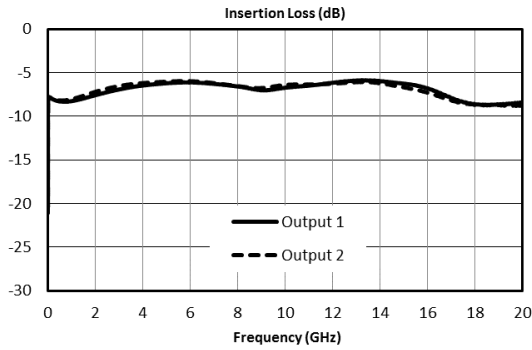


Fig. 7. Common to output port insertion loss

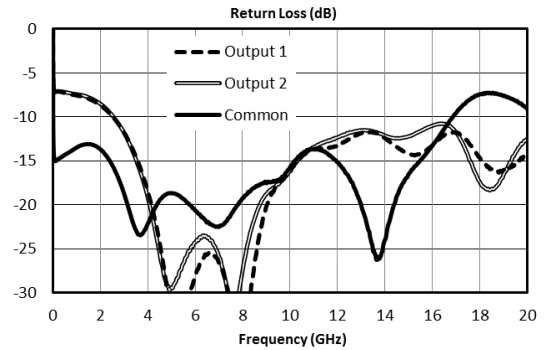


Fig. 8. Return loss for common port and output ports.

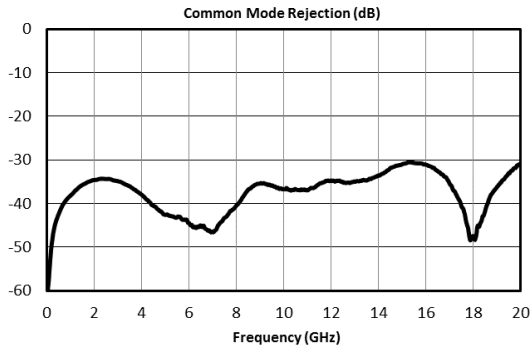


Fig. 9. Common mode rejection.

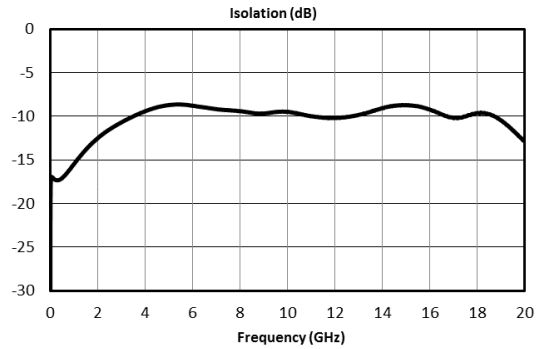


Fig. 10. Isolation between output ports

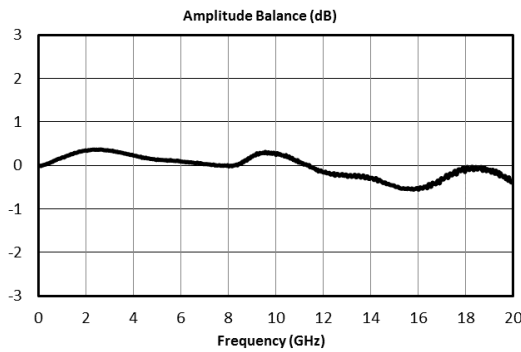


Fig. 11. Amplitude balance between output ports.

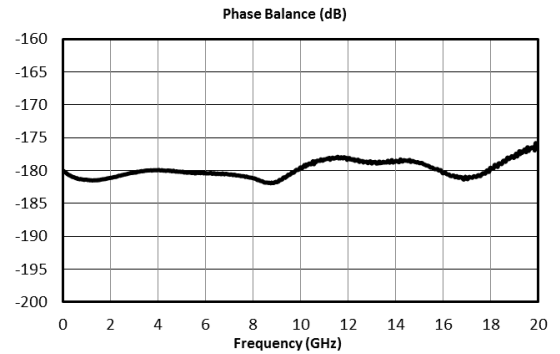


Fig. 12. Phase balance between output ports.

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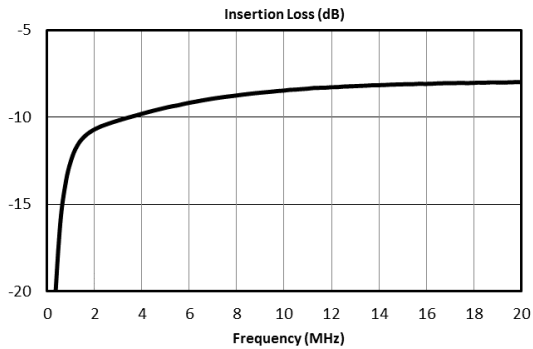
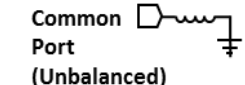
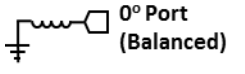
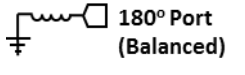


Fig. 13. Low Frequency Insertion Loss

DC Interface

Port	Description	DC Interface Schematic
Common Port / In (Unbalanced)	The common port is DC short to ground.	
Out 1 / 0° Port (Balanced)	The 0° port is DC short to ground.	
Out 2 / 180° Port (Balanced)	The 180° port is DC short to ground.	

Absolute Maximum Ratings	
Parameter	Maximum Rating
DC Current	TBD
RF Power Handling	TBD
Operating Temperature	-55°C to +100°C
Storage Temperature	-65°C to +125°C



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DATASHEET NOTES:

1. Sdd22: differential return loss of the differential port driven with a differential signal
Sdc22: differential return loss of the differential port driven with a common signal
Sds21: insertion loss from a single ended input to a differential output
Scc22: common mode return loss of the differential port driven with a common signal
Scd22: common mode return loss of the differential port driven with a differential signal
Scs21: insertion loss from a single ended input to a common output
Sss11: single ended return loss
Ssd12: insertion loss from a differential signal to single ended output
Ssc12: insertion loss from a common signal to single ended output

Revision History

Revision code	Revision Date	Comment
-	August 2020	Draft

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