Chip Scale Package MMIC 50 GHz 10dB Attenuator

1 Device Overview

1.1 General Description
The ATN10-0050CSP1 is a surface mount GaAs MMIC 10dB attenuator in a chip scale package (CSP). This attenuator is an ideal solution for attenuating a signal and can be used in a wide range of applications. The CSP allows for extreme miniaturization of SMT footprint while providing die-like performance. GaAs MMIC technology provides consistent unit-to-unit performance in a small, low-cost form factor. Compensates for high frequency board losses with a positive gain slope. A 50-ohm match is maintained over the entire operating frequency range.

1.2 Features
- Small 1.5 x 1.5 mm package size
- 10dB attenuation from DC to 50 GHz
- 22dB typical return loss over operating band
- 1W Power Handling
- Low SWaP
- S2P data: ATN10-0050CSP1.s2p

1.3 Applications
- 5G
- Airborne Applications
- Test Equipment
- Amplitude Matching
- Precision Characterization
- High Channel Count Systems

1.4 Functional Block Diagram

1.5 Part Ordering Options

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Attenuation (dB)</th>
<th>Description</th>
<th>Package</th>
<th>Green Status</th>
<th>Product Lifecycle</th>
<th>Export Classification</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATN10-0050CSP1</td>
<td>10</td>
<td>1.5 x 1.5 mm CSP</td>
<td>CSP1</td>
<td>RoHS</td>
<td>Active</td>
<td>EAR99</td>
</tr>
<tr>
<td>EVB-ATN10-0050</td>
<td>10</td>
<td>Connectorized Eval Module</td>
<td>Module</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Refer to our website for a list of definitions for terminology presented in this table.
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Revision History

<table>
<thead>
<tr>
<th>Revision Code</th>
<th>Revision Date</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>April 2022</td>
<td>Datasheet Initial Release</td>
</tr>
<tr>
<td>A</td>
<td>June 2022</td>
<td>Outline Drawings Updated</td>
</tr>
</tbody>
</table>
2 Port Configurations and Functions

2.1 Port Diagram
An x-ray view of the ATN10-0050CSP1 package outline drawing is shown below. The ATN attenuators are symmetrical allowing Port 1 or Port 2 to be used as the input.

![Port Diagram](image)

2.2 Port Functions

<table>
<thead>
<tr>
<th>Port</th>
<th>Function</th>
<th>Description</th>
<th>Equivalent Circuit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1</td>
<td>Input/Output</td>
<td>Pin 1 and pin 2 are DC connected to each other and ground through a T-network of resistors.</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
</tr>
<tr>
<td>Pin 2</td>
<td>Input/Output</td>
<td></td>
<td></td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
<td>SM package ground path is provided through the ground paddle.</td>
<td><img src="image" alt="Equivalent Circuit" /></td>
</tr>
</tbody>
</table>
3 Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum Rating</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Handling, at any Port</td>
<td>1</td>
<td>W</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-55 to +100</td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65 to +125</td>
<td>°C</td>
</tr>
</tbody>
</table>

3.2 Package Information

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Details</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESD</td>
<td>Human Body Model (HBM), per MIL-STD-750, Method 1020</td>
<td>TBD</td>
</tr>
</tbody>
</table>

3.3 Electrical Specifications\(^2\)

The electrical specifications apply at \(T_A=+25^\circ\text{C}\) in a 50Ω system. Typical data shown is for the equalizer in a SM package with a sine wave input applied to port 1.

Min and Max limits are guaranteed at \(T_A=+25^\circ\text{C}\). All bare die are 100% DC tested and visually inspected.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Frequency Range (GHz)</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Insertion Loss (dB)</td>
<td>DC to 30</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>30 to 50</td>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Return Loss (dB)</td>
<td>DC to 40</td>
<td>15</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td></td>
<td>40 to 50</td>
<td>18</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Impedance (Ω)</td>
<td>DC to 50</td>
<td>50</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\(^2\) Attenuator is symmetrical. Reverse measurement is equivalent to forward measurement. All measurements taken in eval and de-embedded to the CSP1 pad interface.
3.4 Typical Performance Plots

3.4.1 Electrical Performance

3 Electrical Performance Data is de-embedded to the CSP package ports

3.4.2 Electrical Performance Over Temperature

4 Evaluation board performance is shown as a proxy for device performance due to fixturing variability over temperature
4 Mechanical Data

4.1 CSP1 Package Outline Drawing

Unless otherwise specified, dimensions are in inches. Tolerances are:

- .X ± .1
- .XXX ± .004

1. Front to back registration to be 50.8µm max.
2. Circuits to be shipped individually.
3. Shaded areas are metalized.
4. Finish: Ni: 0.5 - 2.5 µm
   Pd: 0.02 - 0.15 µm
   Au: 0.003 - 0.015 µm

4.2 CSP1 Package Footprint

- Recommended to have the ground plane flooded. Ground plane are left to PCB designer's discretion.

Ø.010 Plated thru via epoxy filled. Recommended conductive or non-conductive fill, 6 PL. Vias can be added or reduced at PCB designer's discretion.

The landing pattern is to be used on Rogers4003, 0.008" thick, 1/2 Oz Cu.

SM-Package Surface-Mount Landing Pattern
Click here for a DXF of the above layout.
Click here for leaded solder reflow. Click here for lead-free solder reflow.
4.3 EVB Package Outline Drawing

All measurements are typical

Edge Mount Connector
2.40mm Female, 2PL.

Backside Label

Unless otherwise specified, dimensions are in inches. Tolerances are:

| .XX | ±.02 |
| .XXX | ±.005 |