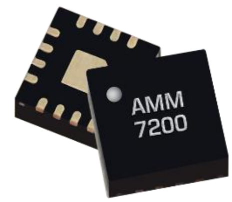
12-46 GHz GaAs Surface Mount LO Driver Amplifier — AMM-7200SM

1. Device Overview

1.1 General Description

The AMM-7200SM is a surface-mount amplifier suitable for use as a single tone driver or general-purpose gain block. It can drive an L or H diode mixer from 12 to 46 GHz, or S diode mixer from 14 to 40 GHz when supplied with 0-10dBm input power. This amplifier also has exceptionally low input and output reflections, and excellent gain flatness in-band. The AMM-7200SM is packaged in a compact 3mm QFN for surface mount integration onto printed circuit boards.



Surface Mount QFN

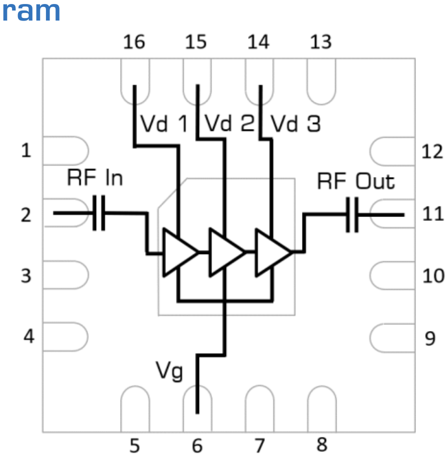
1.2 Features

- +20 dB Small Signal Gain
- Can drive H, L, or S diode mixer
- +20 dBm saturated output power
- Excellent return losses
- Compact 3mm QFN package
- .s2p S-Parameters: EVAL-AMM-7200SM.s2p

1.3 Applications

- Mobile test and measurement equipment
- Radar and satellite communications
- 5G transceivers
- LO driver for Marki L-, H-, and S-diode mixers

1.4 Functional Block Diagram



1.5 Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
AMM-7200SM	3x3 mm Surface Mount	QFN	**RoHS**	Pre-Release	3A001.b.2.d
EVAL-AMM-7200SM	Connectorized Evaluation Fixture	EVAL	**RoHS**	Pre-Release	EAR99

[1] Refer to our website for a list of definitions for terminology presented in this table.

Table of Contents

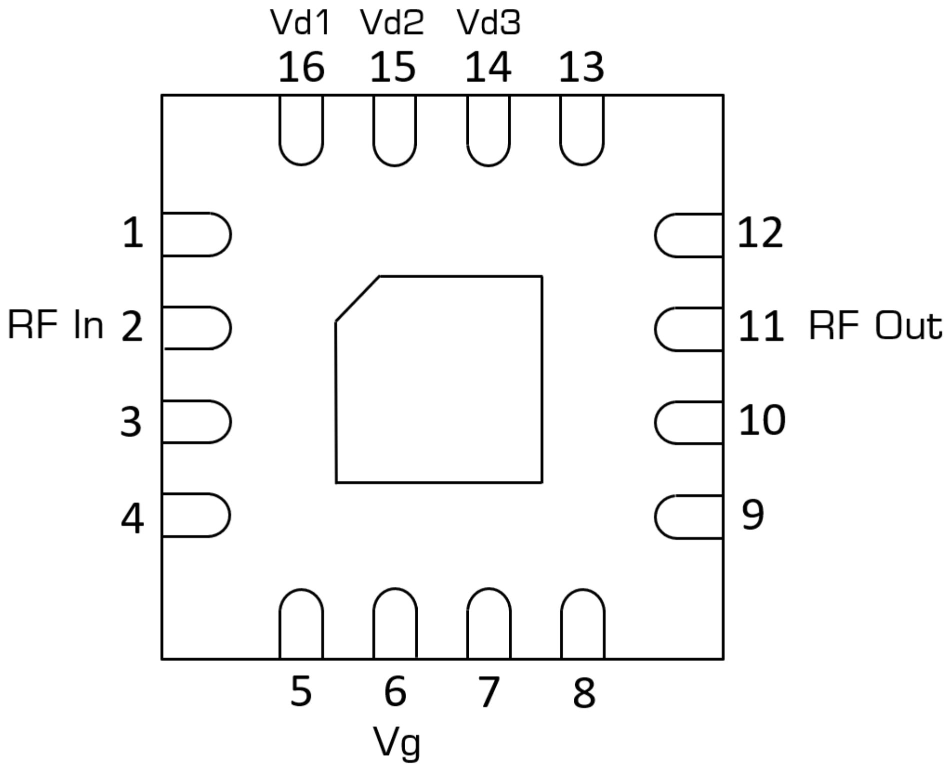
Revision History

Revision Code	Revision Date	Comment
PRE	February 2021	Pre-Release

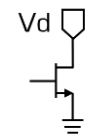
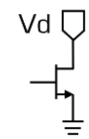
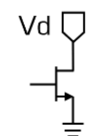
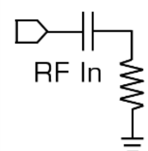
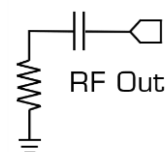
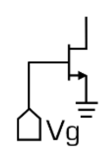
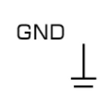
2. Port Configurations and Functions

2.1 Port Diagram

A port diagram of the AMM-7200SM's QFN package is shown below. The pin functions are detailed in section 2.2 of this datasheet.



2.2 Port Functions

Port	Function	Description	Equivalent Circuit for Package
Pin 14[2]	Positive DC Supply V_d	Pins 14 provides +2V to +4V DC voltage to the amplifier's third stage. **Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.**	
Pin 15[2]	Positive DC Supply V_d	Pins 15 provides +2V to +4V DC voltage to the amplifier's second stage. **Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.**	
Pin 16[2]	Positive DC Supply V_d	Pins 16 provides +2V to +4V DC voltage to the amplifier's first stage. **Negative voltage must be supplied to Pin 6 before turning on the positive supply voltage.**	
Pin 2	RF Input	Pin 2 is the RF input of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	
Pin 11	RF Output	Pin 11 is the RF output of the amplifier, and is matched to 50 ohms. It is internally DC blocked.	
Pin 6[3]	Negative DC Supply V_g	Pin 6 provides -0.2V to -0.7V of DC voltage. This must be turned on before turning on the positive supply voltage to Pin 1.	
GND	Ground	Ground paddle and non-connected pins must be connected to a DC/RF ground potential with high thermal and electrical conductivity, and low inductance.	

[2] Pins 14, 15, and 16 may be biased together for ease of use, or individually to adjust overall performance

[3] Pin 6 may be biased with constant DC voltage, or actively biased to produce a fixed Id for consistent performance.

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Power Supply Voltage (Pin 14, 15, 16)	4.5	V
Negative Bias Voltage (Pin 6)	-2	V
RF Input Power	+15	dBm
Operating Temperature	-40 to +85	ºC
Storage Temperature	-65 to +150	ºC
Max Junction Temperature for MTTF > 1E6 Hours	175	ºC

3.2 Package Information

Parameter	Details	Rating
Weight	EVAL Package	31.2g

3.3 Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications (3.5). Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the Electrical Specifications. For limits, above which damage may occur, see Absolute Maximum Ratings (3.1).

	Min	Nominal	Max	Units
T_A, Ambient Temperature	-55	+25	+85	°C
Power Supply DC Voltage	+2	+3	+4	V
Power Supply DC Current[4]	100	180	350	mA
Gate Bias DC Voltage	-0.7	-0.5	-0.2	V
Input Power for Saturation	+5	+10	+15	dBm

3.4 Sequencing Requirements

Turn-on Procedure:

1) Apply <-0.2V to Vg (Pin 6)
2) Apply Vd (Pin 14, 15, 16)

Turn-off Procedure:

1) Turn off Vd (Pin 14, 15, 16)
2) Turn off Vg (Pin 6)

[4] Power Supply DC current is specified as $Id_1 + Id_2 + Id_3$

3.5 Electrical Specifications

The electrical specifications apply at T_A=+25°C in a 50Ω system.

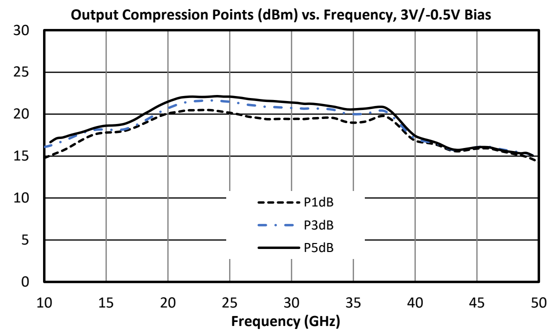
QFNs are 100% RF tested.

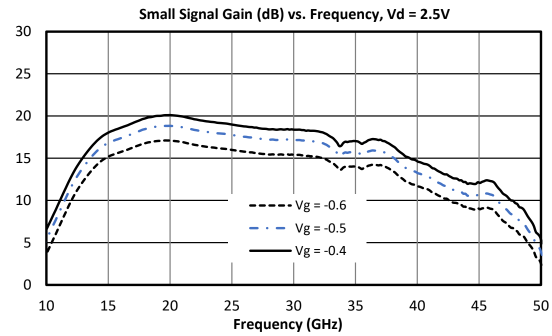
Parameter	Test Conditions	Frequency	Min	Typical	Units
Saturated Output Power[5]	3V/-0.5V bias	12 GHz – 22 GHz		+19	dBm
		22 GHz – 38 GHz	+18	+21	
		38 GHz – 46 GHz		+17	
Small Signal Gain	3V/-0.5V bias, -25 dBm Input Power	12 GHz – 22GHz		16	dB
		22 GHz – 38 GHz	13	16	
		38 GHz – 46 GHz		12	
Input Return Loss		12 GHz – 46 GHz		18	
Output Return Loss		12 GHz – 46 GHz		14	
Reverse Isolation		12 GHz – 46 GHz		52	
Noise Figure	3V/-0.5V Bias	12 GHz – 46 GHz		6.9	
Drain Current[6], Id	3V/-0.4V	-		230	mA
	3V/-0.5V	-		180	
	3V/-0.6V	-		130	
Input IP3 (IIP3)	3V/-0.5V bias, -20 dBm Input Power	12 GHz – 46 GHz		+14	dBm
Output IP3 (OIP3)		12 GHz – 46 GHz		+29	
Output P_{1dB}	3V/-0.5V bias	12 GHz – 46 GHz		+18	
Input Power for Saturation	3V/-0.5V bias	12 GHz – 46 GHz		+15	dBm

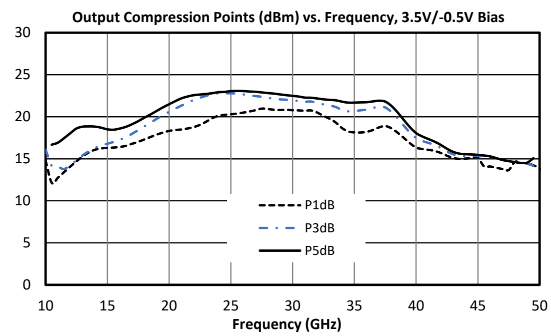
[5] Saturated output power specification defined using the EVAL-APM-7200SM P_{5dB} compression curve shown in section 3.6

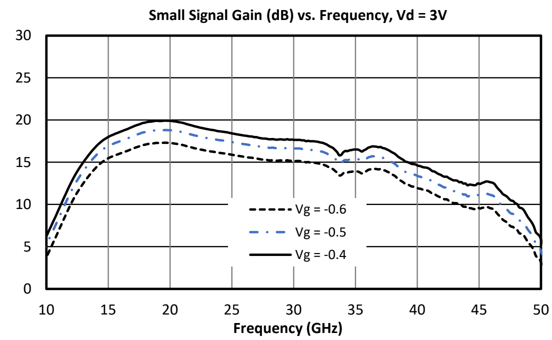
[6] Bias conditions for Id tested with no RF input power. See section 3.6 for DC current vs. RF power. Bias conditions presented as Vd/Vg. Drain current is specified as $Id_1 + Id_2 + Id_3$

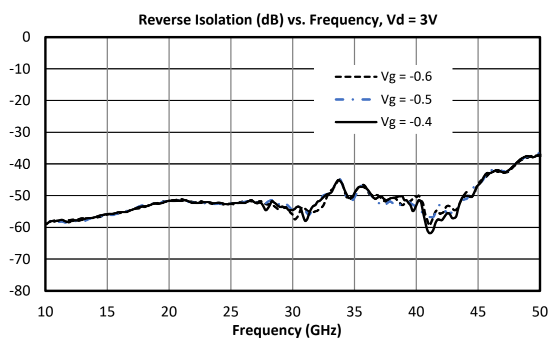
3.6 Typical Performance Plots[7]

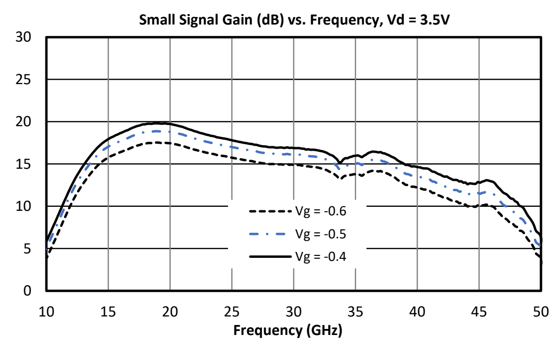


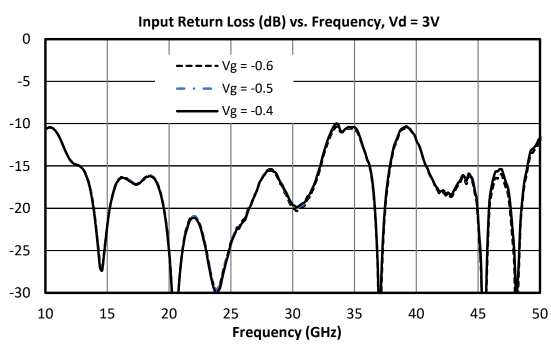


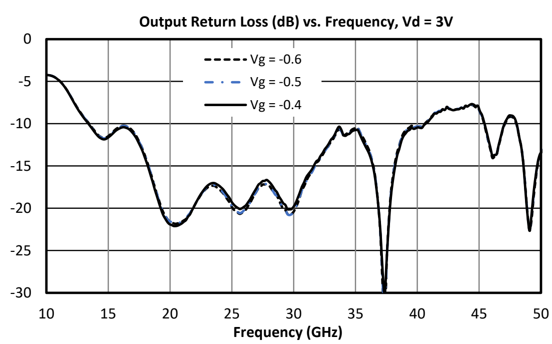




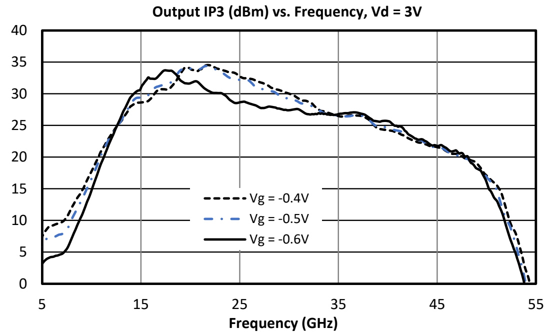


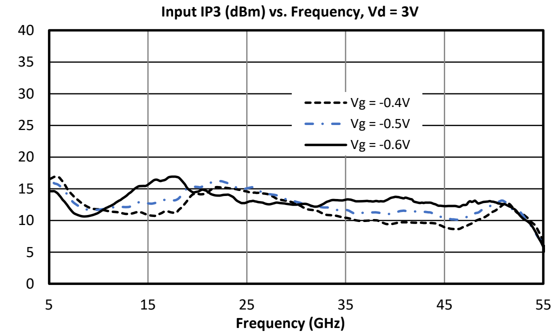


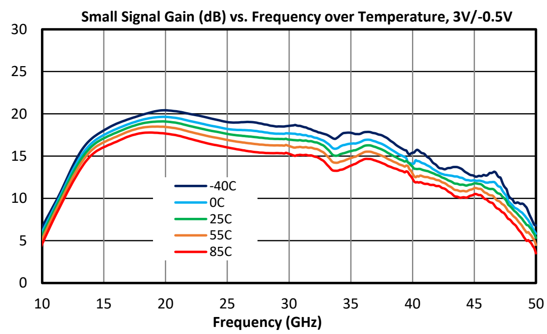


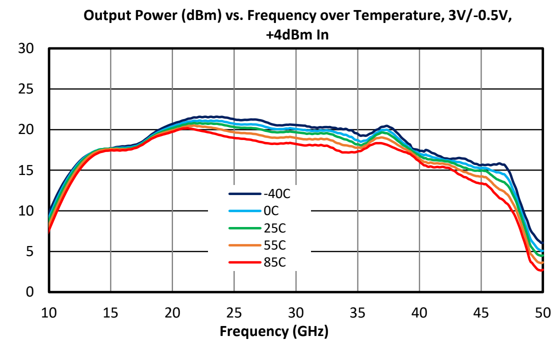


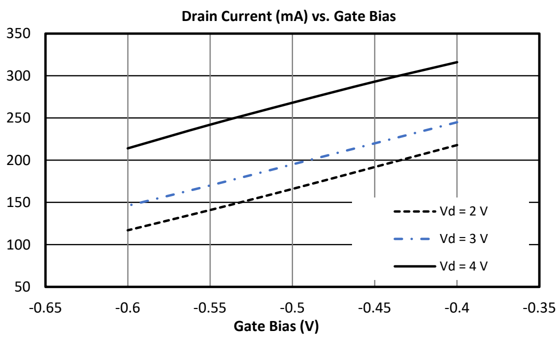
[7] Measurement data taken using the EVAL-AMM-7200SM module.

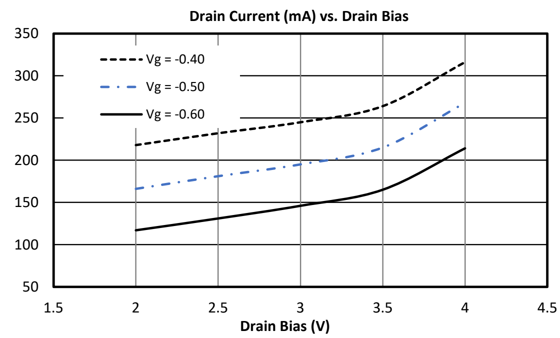


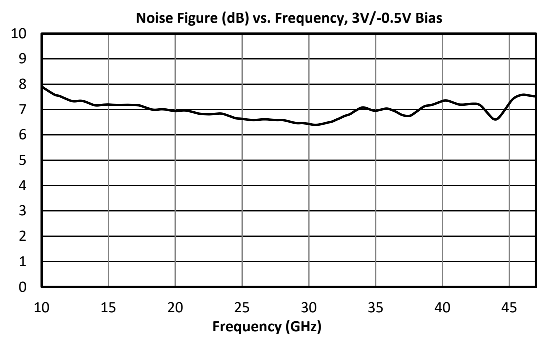


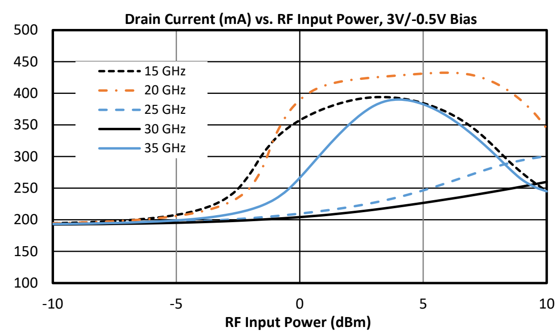








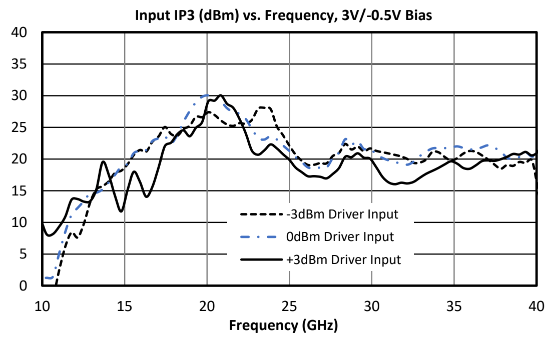


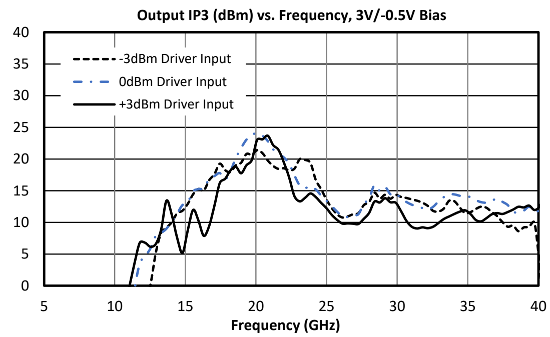


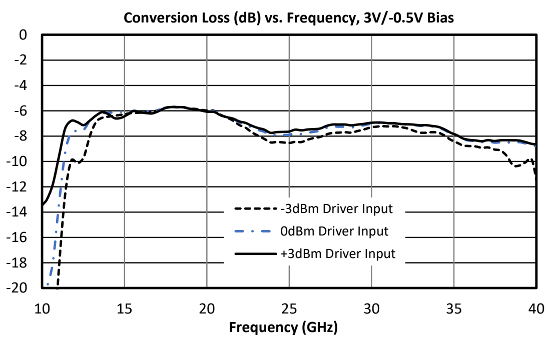
[9]

[9] Drain current is specified as $Id_1 + Id_2 + Id_3$

3.7 Typical Performance Plot of Marki MM1-1140H Using AMM-7200SM as LO Driver[10]







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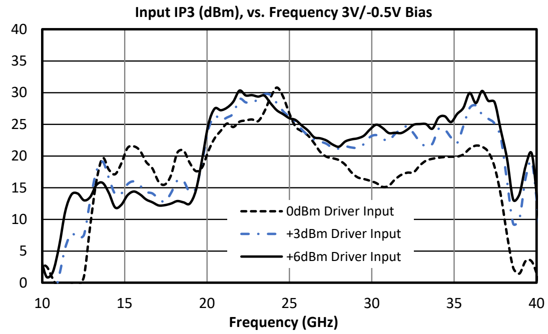
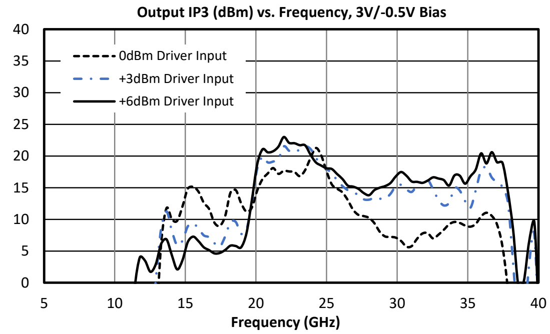
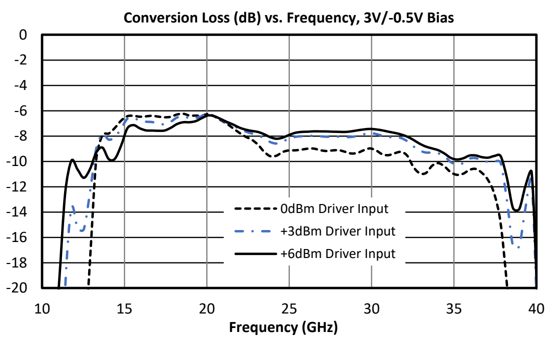
[10] Plots taken using EVAL-AMM-7200SM as LO driver for connectorized MM1-1140H module in configuration A with a 91MHz IF. Power specified is input power to EVAL-AMM-7200SM driver.

3.8 Typical Performance Plot of Marki MM1-1240S Using AMM-7200SM as LO Driver[11]







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[11] Plots taken using EVAL-AMM-7200SM as LO driver for connectorized MM1-1240S module in configuration A with a 91MHz IF. Power specified is input power to EVAL-AMM-7200SM driver.

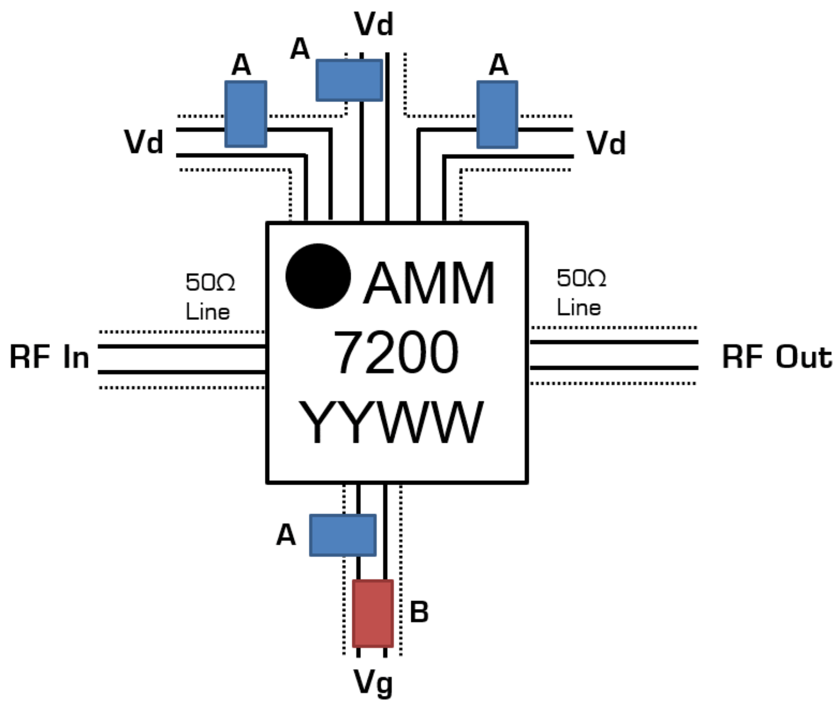
4. Application Information

4.1 Best Practices to Prevent Oscillations

Millimeter-wave amplifiers such as the AMM-7200SM are susceptible to oscillation due to positive feedback either from the bias lines or radiation in metal cavities. To prevent bias line feedback, 0.1µF bypass capacitors should be placed on all DC biasing lines close to the QFN. Additionally, a series resistor should be placed on the gate biasing pin close to the QFN with a value between 10 and 100 ohms (see application circuit in 4.2). Higher resistor values than 100 ohms will lead to excessive drain current draw and possible performance degradation. Radiative feedback can be minimized by placing RF absorbing material in the space between the QFN and the metal cavity.

4.2 Example Application Circuit

Below is the recommended application circuit for the AMM-7200SM:



Designator	Description	Sample Part Number
A	0.1µF 16V 0402 Capacitor	AVX 0402YD104KAT2A
B	10Ω 0402 Resistor	TE CPF0402B10RE1

The three Vd lines are separated to minimize feedback between the transistor's stages. The passive devices should be 0402 or 0201 surface mount. Examples of suitable passive devices would be the AVX 0402YD104KAT2A capacitor and TE CPF0402B10RE1 resistor. In addition to the resistor and capacitor on the gate pin, the layout of the board should be designed to minimize stray coupling between the drain and gate biasing traces on the board. Additionally, the gate biasing pin AMM-7200SM can draw up to 0.5mA at certain combinations of frequency and input power.

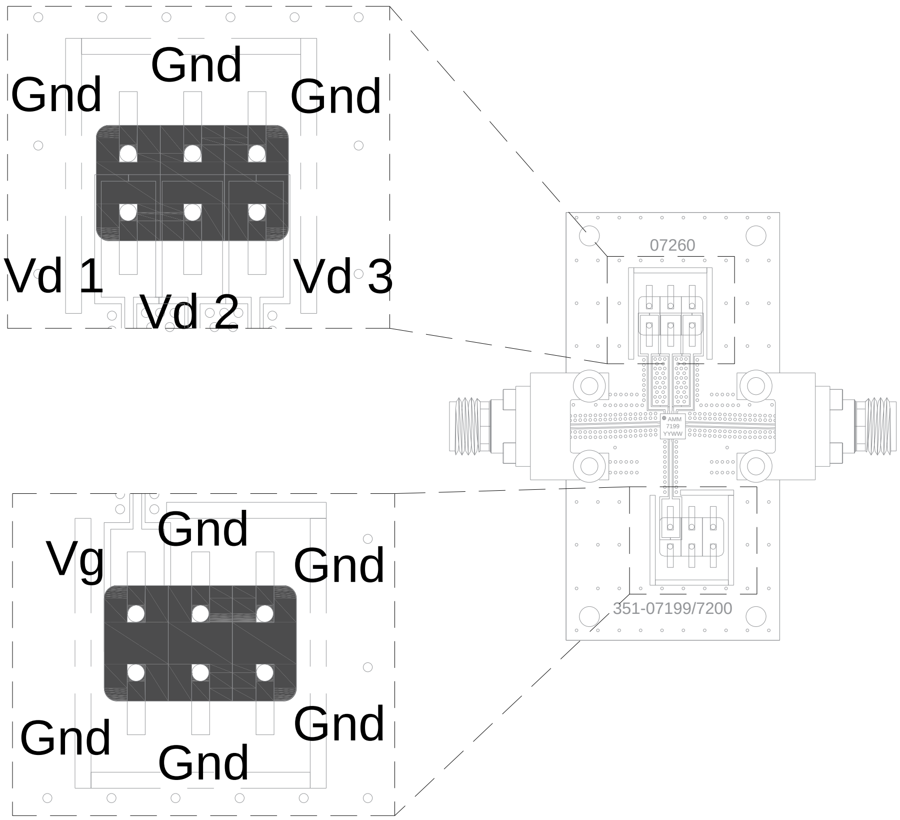
4.3 Constant Current and Constant Voltage Operation

As with most amplifiers utilizing HEMT technology, the AMM-7200SM can be biased with a constant gate and drain voltage, or with a constant drain current by regulating the gate voltage. Using a constant gate and drain voltage for biasing reduces complexity, but has variable current consumption during operation. On the other hand, biasing the gate using a feedback network that samples the drain current minimizes unit-to-unit variation in gain and other parameters.

Under small signal excitation at a fixed temperature, these two approaches are equivalent. However, they will diverge in large signal conditions, where the drain current is affected by the frequency and power of the input signal. In these conditions P1dB, P3dB, and P5dB will be somewhat different, but based on tests with similar parts, they will be within a few dBm of the constant voltage curves.

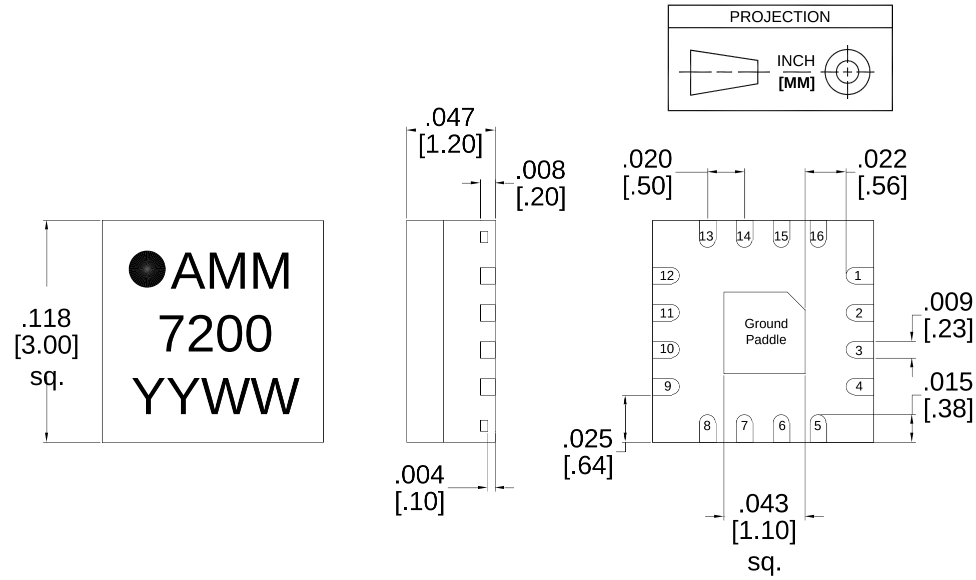
4.3 Header Pinouts

On the EVAL-AMM-7200SM, there are two headers for biasing the drains and gates of the transistors. The pinout of the headers is given with their location on the evaluation board below:



5. Mechanical Data

5.1 SMT Package Outline Drawing

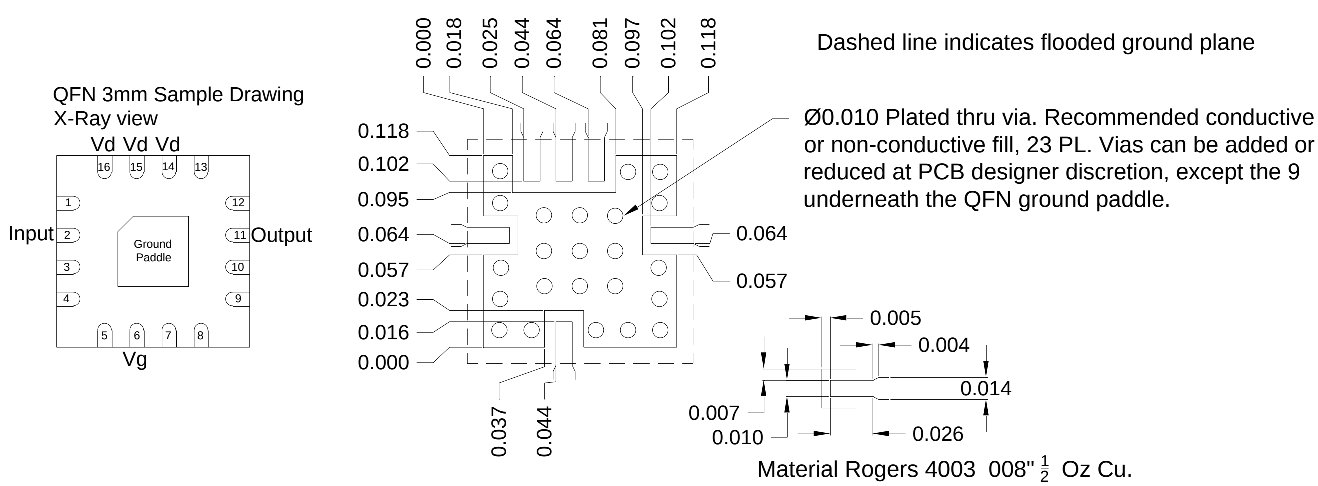


Pin #	Port
1	N/C
2	RF In
3	N/C
4	N/C
5	N/C
6	Vg
7	N/C
8	N/C
9	N/C
10	N/C
11	RF Out
12	N/C
13	N/C
14	Vd 3
15	Vd 2
16	Vd 1

Notes:

1) QFN material is plastic
2) I/O Leads and Die Paddle are 0.05 microns Au over 0.02 microns Pd over 0.5 microns Ni
3) All unconnected pins should be connected to PCB RF ground.

5.2 AMM-7200SM Recommended PCB Footprint



Landing pattern .dxf drawing: Landing Pattern AMM7200SM.dxf

5.3 EVAL Package Outline Drawing