1. Device Overview

1.1 General Description

The ADM3-00001PD is a high-gain, broadband 3-stage amplifier capable of providing +21 dBm output power up to 18 GHz. This amplifier features a flat group delay, fast rise time response, and low noise figure. This product is an unprotected amplifier module intended for lab use.[1]

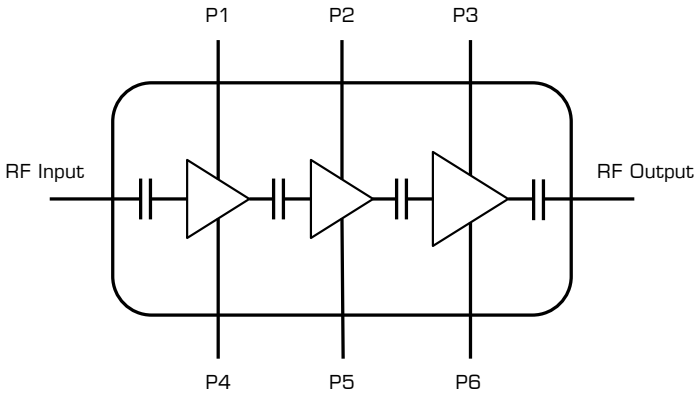
1.2 Features

- +23 dBm output power
- +37 dB gain
- Flat group delay response
- .s2p S-Parameters: ADM3-00001PD

1.3 Applications

- Test and measurement equipment
- LO Driver Amplifier

1.4 Functional Block Diagram



1.5 Part Ordering Options[2]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
ADM3-00001PD	Connectorized Module[3]	PD	**RoHS**	Active	EAR99

[1] See section 1.6 for a complete list of warnings.
[2] Refer to our website for a list of definitions for terminology presented in this table.
[3] Customer-provided heat sink is recommended to maintain proper operating temperature – please contact support for recommendations.

1.6 Warnings

- The ADM3-00001PD is for use in a controlled laboratory environment and is not suitable for use in high reliability applications.
- Module may be catastrophically damaged by heat. Special care must be taken to maintain operating temperature within limits.
- Heat sinking is recommended to maintain proper operating temperature of the amplifier.
- The amplifier may be catastrophically damaged by incorrect sequencing or disruption of the negative supply voltage. Always sequence according to section 3.4.
- Operation of the amplifier without a load or with excessive output reflections can catastrophically damage the module.
- Care must be taken to reduce or eliminate ESD discharge in the test environment.
- Users must rigidly adhere to absolute maximums (3.1) and sequencing requirements (3.4) to prevent catastrophic failure.
- Care must be taken to prevent damage due to excessive DC current, overheating, ESD, and damage due to large output reflections.
- Care must be taken to avoid exceeding negative gate current rating listed in absolute maximums (3.1) to prevent catastrophic failure.

Table of Contents

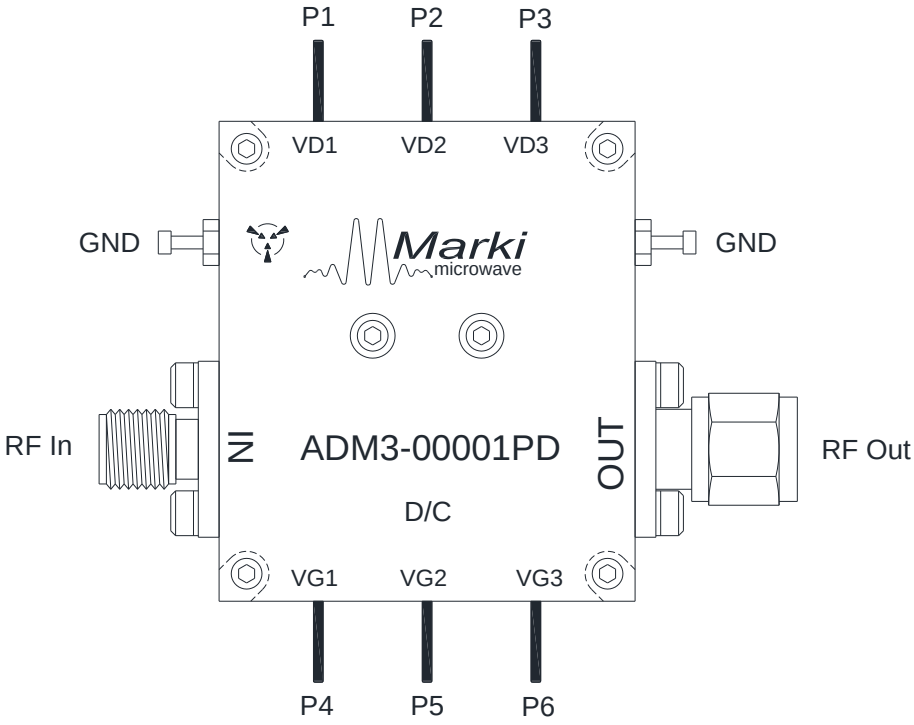
Revision History

Revision Code	Revision Date	Comment
-	December 2022	Datasheet Initial Release

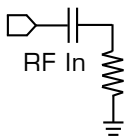
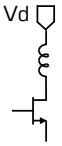
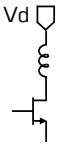
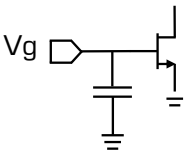
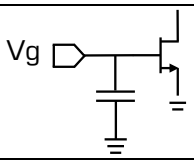
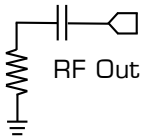
2. ADM3-00001PD Port Configurations and Functions

2.1 ADM3-00001PD Port Diagram

A port diagram of the ADM3-00001PD is shown below.



2.2 ADM3-00001PD Port Functions

Pin	Function	Description	Equivalent Circuit for Package
RF In	RF Input	The RF input port of the amplifier is matched to 50Ω and has built-in DC blocking capacitors.	
P1, P2	Vd1, Vd2	P1 and P2 are the positive DC voltage supply pins for the drains on the 1st and 2nd stage amplifiers, recommended +5V. **Vg1/Vg2 must be applied to P4/P5 prior to application of Vd1/Vd2 on P1/P2!**	
P3	Vd3	P3 is the positive DC voltage supply pin for the drain on the 3rd stage amplifier, recommended +7V. **Vg3 must be applied to P6 prior to application of Vd3 on P3!**	
P4, P5	Vg1, Vg2	P4 and P5 are the negative DC voltage bias pins for the gates on 1st and 2nd stage amplifiers, recommended 0V. **Must be applied prior to application of Vd1/Vd2 on P1/P2!**	
P6	Vg3	P6 is the negative DC voltage bias pin for the gate on the 3rd stage amplifier, recommended -0.3V. **Must be applied prior to application of Vd3 on P3!**	
RF Out	RF Output	The RF output port of the amplifier is matched to 50Ω and has built-in DC blocking capacitors.	
GND	Ground	A single or both GND lugs must be connected to a DC/RF ground potential with high thermal and electrical conductivity. Ensure that the ground voltage is a common reference potential to all DC power supplies.	GND 

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may become inoperable or have a reduced lifetime. Reliability limits are individual, instantaneous catastrophic limits only. Functional operation limits are indicated below. Operation of the device at multiple absolute maximum limits or for extended periods at a single limit can cause degradation and damage to the device.

Parameter	Maximum Rating	Units
P1 & P2 Drain Supply Voltage (Vd1, Vd2)	+7	V
P1 & P2 Positive Bias Current (Id1, Id2)	150	mA
P3 Drain Supply Voltage (Vd3)	+8	V
P3 Positive Bias Current (Id3)	230	mA
P4 & P5 Gate Bias Voltage (Vg1, Vg2)	0	V
P6 Gate Bias Voltage (Vg3)	0	V
P4, P5, P6 Gate Bias Current (Ig1, Ig2, Ig3)	0.5	mA
RF Input Power	-5	dBm
Operating Temperature	-40 to +55	°C
Storage Temperature	-55 to +125	°C
θ_{JA}, Junction to Ambient Thermal Resistance	10	°C/W

3.2 Package Information

Parameter	Details	Rating
Weight	AMD3-00001PD	41 g

3.3 Recommended Operating Condition

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications.

Recommended Operating Conditions	Min	Nominal	Max	Units
T_A, Ambient Temperature	-40	+25	+55	°C
Power Supply DC Voltage (Vd1, Vd2)	3	5	6.5	V
Power Supply DC Current (Id1, Id2)[3]		120	140	mA
Power Supply DC Voltage (Vd3)	3	7	7.5	V
Power Supply DC Current (Id3)[2]		100	220	mA
Gate DC Voltage (Vg1, Vg2)	-0.5	-0.3	0	V
Gate DC Current (Ig1, Ig2)[2]		0	0.1	mA
Gate DC Voltage (Vg3)	-0.5	-0.3	0	V
Gate DC Current (Ig3)[2]		0	0.1	mA
Input Power for Saturation		-10	-5.5	dBm

3.4 Sequencing Requirements

Supply pin sequencing is required to power up or power down the amplifier. The amplifier must have an output load connected during operation.

Turn-on:

1. Ensure RF Out Port is connected to load.
2. Apply -0.3V to port P4 (Vg1) and port P5 (Vg2) and apply -0.3V to port P6 (Vg3).
    a. Gate bias pins can be applied simultaneously.
3. Apply 5V to port P1 (Vd1) and port P2 (Vd2) and apply 7V to port P3 (Vd3).
    a. Drain bias pins can be applied simultaneously.
4. Apply RF power to RF In Port.

Turn-off:

1. Turn off RF power.
2. Remove voltage from port P1 (Vd1), port P2 (Vd2), and port P3 (Vd3).
    a. Drain bias pins can be removed simultaneously.
3. Remove voltage from port P4 (Vg1), port P5 (Vg2), and port P6 (Vg3).
    a. Gate bias pins can be removed simultaneously.
4. Remove load from RF Out Port.

[3] Recommended operating current conditions without RF input applied.

3.5 Electrical Specifications

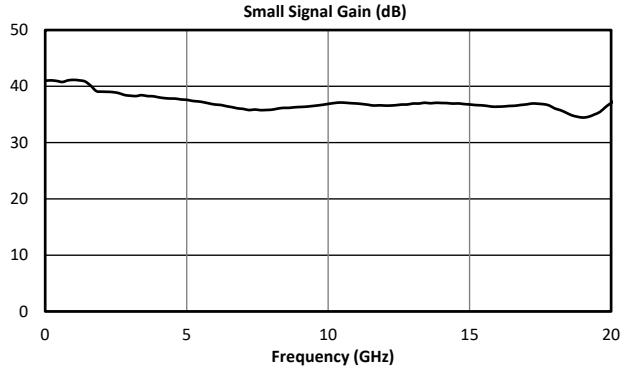
Electrical specifications apply at Vd1=Vd2=5V, Vd3=7V, Vg1=Vg2=0V, Vg3=-0.3V in a 50Ω system at T_A=+25° unless otherwise specified.

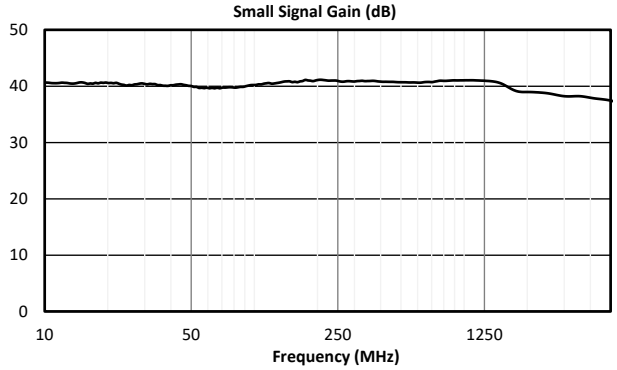
Min and Max limits apply only to our connectorized units and are guaranteed at T_A=+25°C

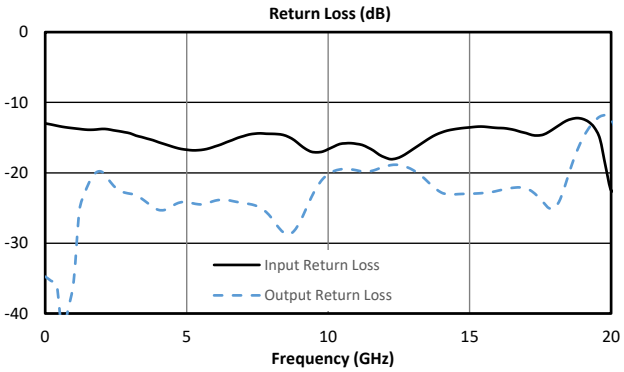
Parameter	Test Conditions	Frequency	Min	Typical	Units
Saturated Output Power	Characterization Bias, Pin = -5 dBm	300 kHz – 18 GHz	18	23	dBm
Small Signal Gain	Vd1, Vd2 = 5V Vd3 = 7 V Vg1, Vg2 = 0V Vg3 = -0.3 V Pin = -40 dBm		32	37	dB
Input Return Loss				15	
Output Return Loss				23	
Reverse Isolation				75	
Noise Figure				5	
Input IP3	Characterization Bias, Pin = -40 dBm per tone, 10 MHz tone spacing			-6	dBm
Output IP3				+31	
Output P1dB	Characterization Bias			+19.5	
Input Power for Saturation				-10	
Rise Time	Characterization Bias, 10 MHz, 0.15Vpp square wave input			44	ps

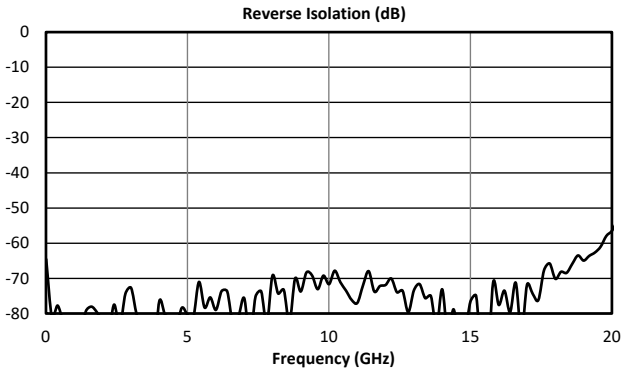
3.6 ADM3-00001PD Typical Performance Plots

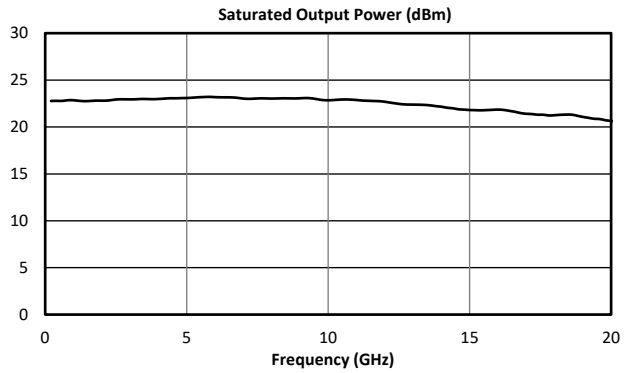
Typical performance is characterized Vd1=Vd2=5V, Vd3=7V, Vg1=Vg2=0V, Vg3=-0.3V in a 50Ω system at T_A=+25°C.

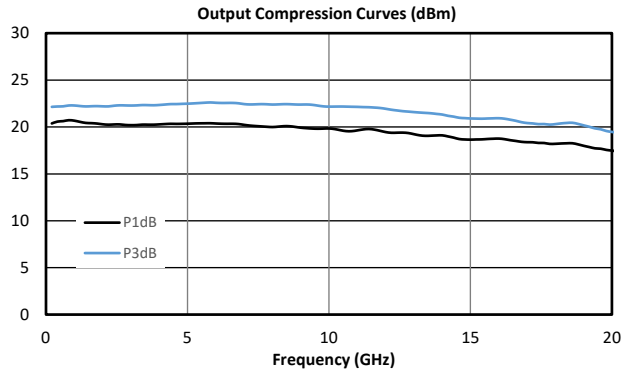


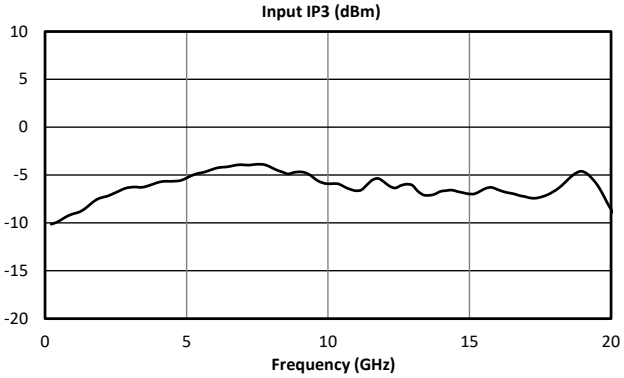


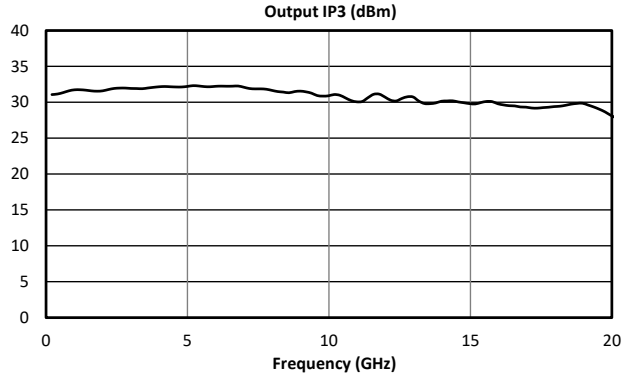


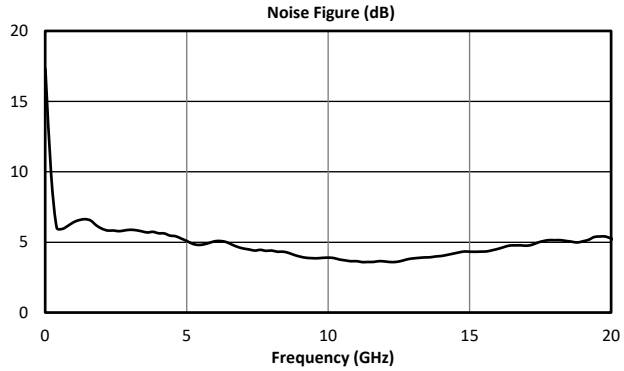


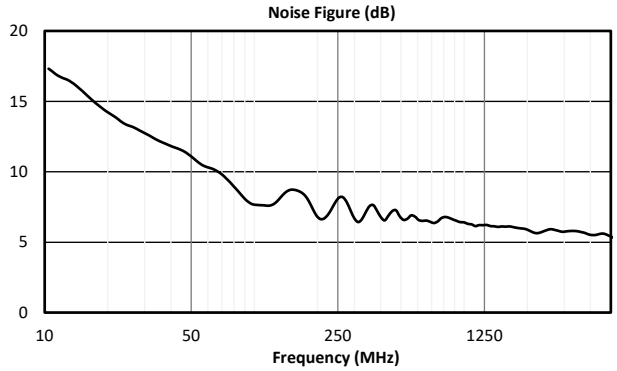


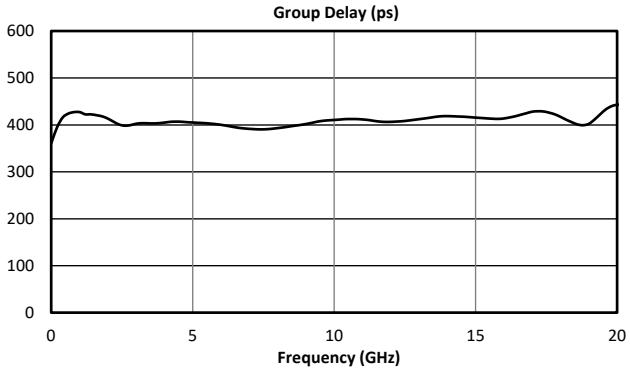






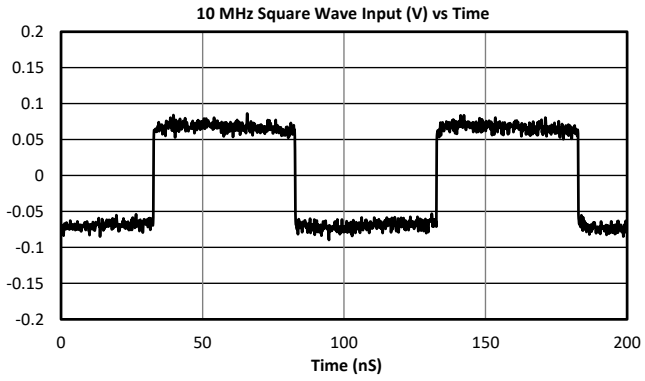


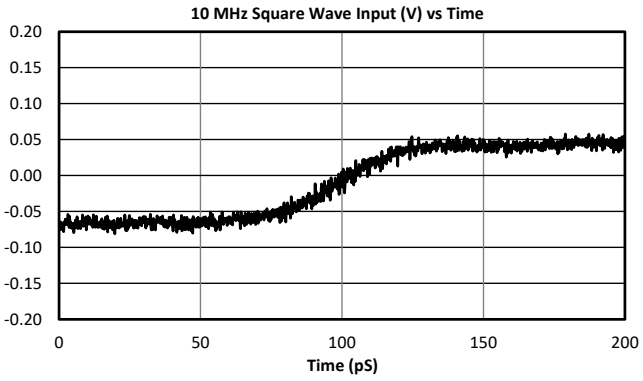


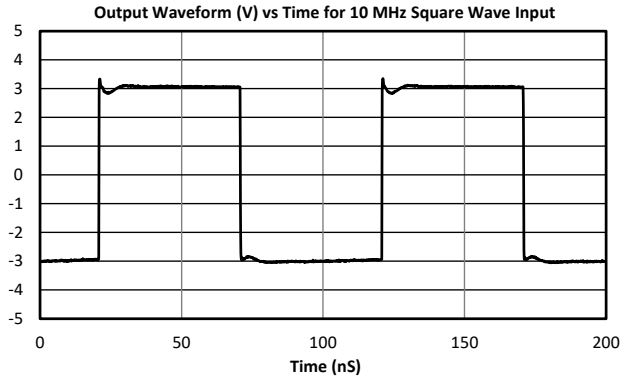


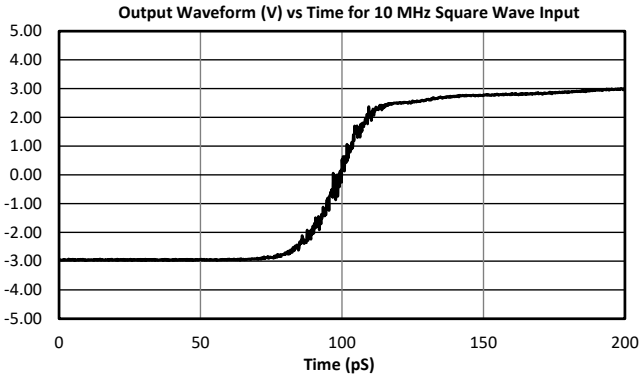
3.7 ADM3-00001PD Time Domain Plots

Typical performance is characterized at Vd1=Vd2=5V, Vd3=7V, Vg1=Vg2=0V, Vg3=-0.3V in a 50Ω system at T_A=+25°C.



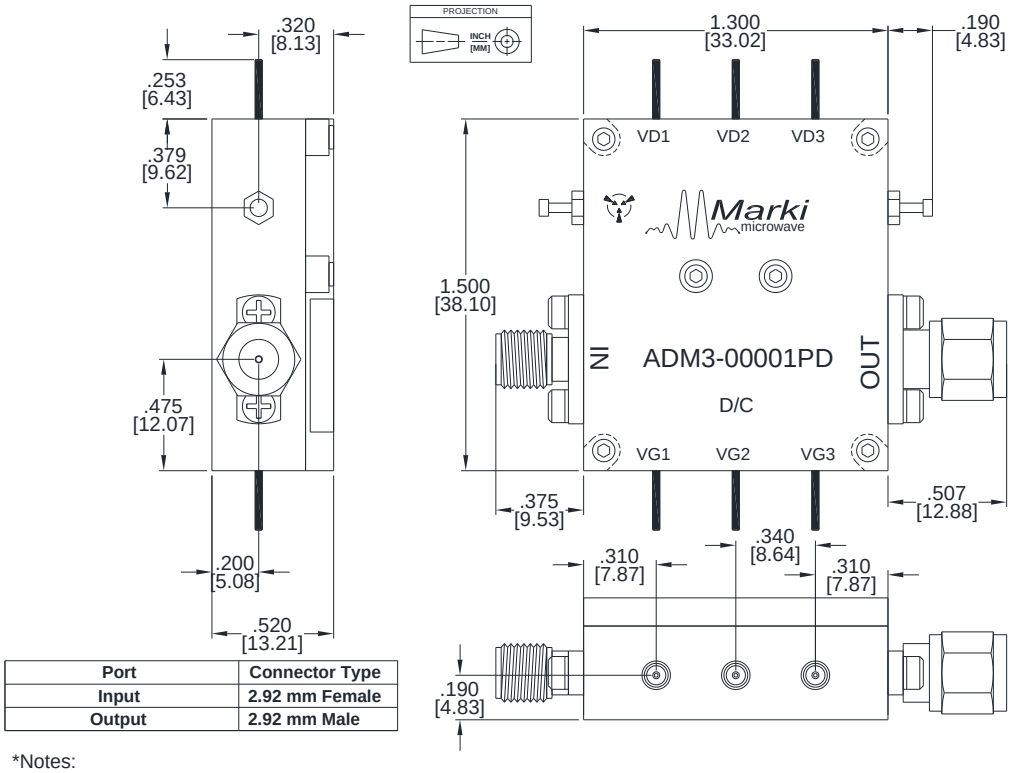






4. Mechanical Data

4.1 ADM3-00001PD Package Outline Drawing



Port	Connector Type
Input	2.92 mm Female
Output	2.92 mm Male

*Notes:
1. All measurements are typical.
2. Ground lug and bias pins are solderable.