BROADBAND DISTRIBUTED AMPLIFIER

ADM-0026-5931SM

The ADM-0026-5931SM is a broadband, power efficient GaAs PHEMT distributed amplifier in a 4mm QFN surface mount package. The ADM-0026-5931SM is designed to provide optimal LO drive for T3 mixers. Typically, ADM-0026-2931SM provides 10.5 dB gain and +16 dBm saturated output power while requiring only 75 mA of current. T3 linearity is enhanced by ADM-0026-5931’s extended high frequency gain and lower harmonic generation when compared to other distributed amplifiers in our catalog. The amplifier can be biased with internal circuitry, or with an external bias network for lower voltage and single supply operation. Additional applications include amplification of clock signals and general purpose driver requirements in electronic warfare and test and measurement.

Features

- Optimized for use as a T3 LO buffer amplifier
- Suitable for driving L, M, and I diode mixers
- Optional Positive Only Bias or Internal Bias Operation
- +16 dBm typical saturated output power
- Broadband 50 Ω Matching
- Unconditionally Stable

Electrical Specifications - Specifications measured in a 50-Ohm system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Frequency (GHz)</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input for Saturated Output (dBm)</td>
<td>DC to 26.5</td>
<td>+5</td>
<td>+10</td>
<td>+12</td>
</tr>
<tr>
<td>Output 1 dB Compression (dBm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Saturated Output Power with negative bias (dBm)</td>
<td></td>
<td></td>
<td></td>
<td>+14</td>
</tr>
<tr>
<td>Small Signal Gain with negative bias (dB)</td>
<td></td>
<td>+16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Return Loss (dB)</td>
<td></td>
<td>10.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Return Loss (dB)</td>
<td></td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Noise Figure (dB)</td>
<td></td>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Third Order Output Intercept Point (dBm)</td>
<td></td>
<td>5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bias Requirements, Internal (mA)</td>
<td>Vd: +10.0 to +12.0 / Vg:-0.25 Volts</td>
<td>25</td>
<td></td>
<td></td>
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<tr>
<td>Bias Requirements, External (mA)</td>
<td>Vd: +5.0 to +7.0 / Vg:-0.25 Volts</td>
<td>80</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vd: +5.0 to +7.0 / Vg: 0 Volts</td>
<td>75</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vd: +5.0 to +7.0 / Vg: 0 Volts</td>
<td>100</td>
<td></td>
<td></td>
</tr>
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</table>

Part Number Options

<table>
<thead>
<tr>
<th>Model Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADM-0026-5931SM (OBS)</td>
<td>Surface Mount 4mm QFN</td>
</tr>
<tr>
<td>EVAL4-ADM-5931 (OBS)</td>
<td>Connectorized Evaluation Fixture</td>
</tr>
</tbody>
</table>

1 Note: For port locations and I/O designations, refer to the drawings on pages 2, 8,11, and 12 of this document.

GaAs MMIC devices are susceptible to Electrostatic Discharge. Use proper ESD precautions when handling these items.

Marki microwave

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4/15/19

NOTE: This product is obsolete. Please see this letter for more information.
Functional Diagram and Application Circuit – External Positive Bias (Pin 16 Output with Bias Tee)

**Biasing and Operation**

**RF In / RF Out** – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors or bias tees are required.

**Vg** – Negative gate voltage is optional to improve lifetime of the amplifier and reduce current consumption. Harmonic generation is also significantly affected by the negative gate voltage level. The amplifier is designed for optimal performance when the negative gate voltage is tuned such that the positive bias supply is 75 mA. It may be supplied through pin 11 or through the RF input on pin 4.

**Vd** – Bias supply supplied to Vd through pin 16 should be voltage limited below 9 V and current limited below 200 mA at all times. The operational bias voltage should be between 5 V and 7 V for full gain, efficiency, and linearity. In general gain, linearity, and output power will increase marginally with increased voltage from 5 to 7 V.

**Optional Bias Circuitry** – The resistor and capacitor on the Vd and Vg lines (pads 21, 23, and 11) prevent low frequency oscillation. These components are not required in bias circuits with sufficient low frequency loss. Designers should experiment to determine if they are necessary.

**DC/RF Ground** – The ground paddle of the QFN should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.
BROADBAND DISTRIBUTED AMPLIFIER

ADM-0026-5931SM

Frequency DC to 26.5 GHz

Typical Performance – Positive Only (+3 to +7V) External Bias (Pin 16 Output), Grounded Gate (Pin 11)
Typical Performance – Positive Only (+3 to +7V) External Bias (Pin 16 Output), Grounded Gate (Pin 11), continued

Even Harmonic Generation (dBm) +10 dBm Input

Odd Harmonic Generation (dBm) +10 dBm Input

Output P1dB (dBm)

Group Delay (ps)

Noise Figure (dB)

Current Consumption (mA) with 10 GHz Input

Vg = -0V, Pin = -10 dBm
Vg = -0V, Pin = +10 dBm
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ADM-0026-5931SM

Frequency DC to 26.5 GHz

Typical Performance – +3 to +7V External Bias (Pin 16 Output), -0.25 Negative Bias (Pin11)

Small Signal Gain (dB)

Frequency (GHz)

+7 Volt/-0.25 Volt Bias
+3 Volt/-0.25 Volt Bias

Small Signal Gain (dB) over Temperature

Frequency (GHz)

-55°C, +7 Volt/-0.25 Volt Bias
+25°C, +7 Volt/-0.25 Volt Bias
+85°C, +7 Volt/-0.25 Volt Bias

Saturated Output Power (dBm)

Frequency (GHz)

+7 Volt/-0.25 Volt Bias
+3 Volt/-0.25 Volt Bias

Reverse Isolation (dB)

Frequency (GHz)

+7 Volt/-0.25 Volt Bias

Input IP3 (dBm)

Frequency (GHz)

+7 Volt/-0.25 Volt Bias
+3 Volt/-0.25 Volt Bias

Output IP3 (dBm)

Frequency (GHz)

+7 Volt/-0.25 Volt Bias
+3 Volt/-0.25 Volt Bias
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ADM-0026-5931SM
Frequency DC to 26.5 GHz

Typical Performance – +3 to +7V External Bias (Pin 16 Output), -0.25 Negative Bias (Pin 11) continued

Input Small Signal Return Loss (dB)
-25 -20 -15 -10 -5 0 5 10 15 20 25 30 Frequency (GHz)
- Input, +7 Volt/-0.25 Volt Bias
- Input, +3 Volt/-0.25 Volt Bias

Input Small Signal Return Loss (dB) over Temperature
-55°C, +7 Volt/-0.25 Volt Bias
+25°C, +7 Volt/-0.25 Volt Bias
+85°C, +7 Volt/-0.25 Volt Bias

Output Small Signal Return Loss (dB)
-25 -20 -15 -10 -5 0 5 10 15 20 25 30 Frequency (GHz)
- Output, +7 Volt/-0.25 Volt Bias
- Output, +3 Volt/-0.25 Volt Bias

Output Small Signal Return Loss (dB) over Temperature
-55°C, +7 Volt/-0.25 Volt Bias
+25°C, +7 Volt/-0.25 Volt Bias
+85°C, +7 Volt/-0.25 Volt Bias

Even Harmonic Generation (dBm) +10 dBm Input
- +7 Volt/-0.25 Volt Bias, Second Harmonic
- +3 Volt/-0.25 Volt Bias, Second Harmonic
- +7 Volt/-0.25 Volt Bias, Fourth Harmonic
- +3 Volt/-0.25 Volt Bias, Fourth Harmonic

Odd Harmonic Generation (dBm) +10 dBm Input
- +7 Volt/-0.25 Volt Bias, Third Harmonic
- +3 Volt/-0.25 Volt Bias, Third Harmonic
- +7 Volt/-0.25 Volt Bias, Fifth Harmonic
- +3 Volt/-0.25 Volt Bias, Fifth Harmonic
BROADBAND DISTRIBUTED AMPLIFIER

ADM-0026-5931SM
Frequency DC to 26.5 GHz

Typical Performance – +3 to +7V External Bias (Pin 16 Output), -0.25 Negative Bias (Pin 11) continued

![Graph of Output P1dB (dBm) vs Frequency (GHz)]

-10 0 5 10 15 20 25 30
0 5 10 15 20 25 30

-7 Volt/-0.25 Volt Bias
+3 Volt/-0.25 Volt Bias

![Graph of Group Delay (ps) vs Frequency (GHz)]

-10 0 5 10 15 20 25 30
0 25 50 75 100 125

-7 Volt/-0.25 Volt Bias
+3 Volt/-0.25 Volt Bias

![Graph of Noise Figure (dB) vs Frequency (GHz)]

-10 0 5 10 15 20 25 30
2 3 4 5 6 7 8

-7 Volt/-0.25 Volt Bias
+3 Volt/-0.25 Volt Bias

![Graph of Current Consumption (mA) with 10 GHz Input vs Vd (V)]

-10 0 5 10 15 20 25 30
2 3 4 5 6 7 8

-7 Vg=-0.25V, Pin=-10 dBm
+3 Vg=-0.25V, Pin=+10 dBm

Functional Diagram and Application Circuit – Internal Positive Bias Tee (Pin 21)

**RF In / RF Out** – Input and output signals should be connected by 50 ohm microstrip or coplanar traces to well matched 50 ohm sources and loads. DC blocking capacitors are required.

**Vg** – Recommended bias on this pin is -0.1 to -0.3 Volts. Harmonic generation is significantly affected by the negative gate voltage level. The amplifier is designed for optimal performance when the negative gate voltage is tuned such that the positive bias supply is 112 mA. It may be supplied through pin 11 or through the RF input on pin 4.

**Vd** – Bias supply on Vd should be voltage limited below 13 V and current limited below 200 mA at all times. The operational bias voltage should be between 10 V and 12 V for full gain, efficiency, and linearity. In general, gain, linearity, and output power will increase marginally with increased voltage from 10 V to 12 V. When the internal positive bias tee is used, pin 23 is left DC and RF open.

**Optional Bias Circuitry** – The resistor and capacitor on the Vd and Vg lines (pads 21, 23, and 11) prevent low frequency oscillation. These components are not required in bias circuits with sufficient low frequency loss. Designers should experiment to determine if they are necessary.

**DC/RF Ground** – The ground paddle of the QFN should be connected to a low noise RF and DC ground with very low electrical and thermal resistance for high frequency operation and thermal heat sinking.
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Frequency DC to 26.5 GHz

Typical Performance – +9 to +12V Internal Bias (Pin 21), -0.25 Negative Bias (Pin 11)

- Small Signal Gain (dB)
- Saturated Output Power (dBm)
- Reverse Isolation (dB)
- Small Signal Return Loss (dB)
- Input IP3 (dBm)
- Output IP3 (dBm)

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ADM-0026-5931SM
Frequency DC to 26.5 GHz

Typical Performance – +9 to +12V Internal Bias (Pin 21), -0.25 Negative Bias (Pin11), continued

Even Harmonic Generation (dBm) +10 dBm Input

Odd Harmonic Generation (dBm) +10 dBm Input

Input P1dB (dBm)

Output P1dB (dBm)

Group Delay (ps)

Noise Figure (dB)

Current Consumption (mA) with 10 GHz Input

Vg= -0.25V, Pin= -10 dBm
Vg= -0.25V, Pin= +10 dBm

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Frequency DC to 26.5 GHz

Substrate material is Ceramic.
I/O Leads and Ground Paddle are 1.4±0.6 microns (55±24 micro-inches) Au over 1.3 microns (51 micro-inches) Ni.
All unconnected pads should be connected to PCB RF ground.

QFN-Package Surface-Mount Landing Pattern
Click here for a DXF of the above layout.
Click here for leaded solder reflow.  Click here for lead-free solder reflow.
### Pin Descriptions

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Function</th>
<th>Description</th>
<th>Interface Schematic</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-3, 5-10, 12-15, 17-20, 22, 24</td>
<td>NC</td>
<td>These pins are not connected internally. Datasheet performance is tested with NC pins grounded.</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>RF in</td>
<td>This pin is DC coupled and matched to 50 Ω.</td>
<td>RF in</td>
</tr>
<tr>
<td>11</td>
<td>Vg</td>
<td>Gate control for the amplifier. External decoupling resistor/capacitor is required.</td>
<td>Vg</td>
</tr>
<tr>
<td>16</td>
<td>RF out</td>
<td>This pad is DC coupled and matched to 50 Ω.</td>
<td>RF out</td>
</tr>
<tr>
<td>21</td>
<td>Vd</td>
<td>Power supply voltage for the amplifier. External decoupling resistor/capacitor is required.</td>
<td>Vd</td>
</tr>
<tr>
<td>23</td>
<td>Vd2</td>
<td>This pin is left open for Internal Vd Bias. This pin is connected to Pin 21 (Vd) for external bias (pin 16 with bias tee).</td>
<td></td>
</tr>
<tr>
<td>Paddle</td>
<td>GND</td>
<td>Ground pad should be connected to RF/DC ground with low electrical and thermal resistance.</td>
<td>GND</td>
</tr>
</tbody>
</table>

### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Maximum Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Positive Bias Voltage – External Bias Tee</td>
<td>9 V</td>
</tr>
<tr>
<td>Positive Bias Voltage – Internal Bias Tee</td>
<td>13 V</td>
</tr>
<tr>
<td>Positive Bias Current</td>
<td>150 mA</td>
</tr>
<tr>
<td>Negative Bias Voltage</td>
<td>-2 V</td>
</tr>
<tr>
<td>Negative Bias Current</td>
<td>2 mA</td>
</tr>
<tr>
<td>RF Input Power</td>
<td>+18 dBm</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>875 mW</td>
</tr>
<tr>
<td>Thermal Resistance, θjc</td>
<td>1.462 C/W</td>
</tr>
<tr>
<td>ESD (Human Body Model)</td>
<td>Class 0</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>-55°C to +85°C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>-65°C to +150°C</td>
</tr>
</tbody>
</table>
The evaluation module follows Marki standard assembly and evaluation procedures to give optimal performance for datasheet characterization. Actual QFN performance will depend on substrate material, bypass capacitors, resistors, connectors, quality of bias current/voltage source, and assembly process.

### Evaluation Board Bill of Materials

<table>
<thead>
<tr>
<th>Item</th>
<th>Description/Part Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>Connectors</td>
<td>Southwest 214-510SF</td>
</tr>
<tr>
<td>Bias Pins</td>
<td>Kovar</td>
</tr>
<tr>
<td>Housing</td>
<td>Aluminum</td>
</tr>
<tr>
<td>Circuit</td>
<td>.008 Thick Rogers 4003</td>
</tr>
<tr>
<td>0.1 uF Capacitor</td>
<td>AVX 0402YD104KAT2A</td>
</tr>
<tr>
<td>10 Ω Resistor</td>
<td>Venkel CR0201-20W-100JT</td>
</tr>
<tr>
<td>ADM 5931</td>
<td>ADM-0026-5931SM</td>
</tr>
</tbody>
</table>

**DATA SHEET NOTES:**

1. Specifications are subject to change without notice. Contact Marki Microwave for the most recent specifications and data sheets.

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