Two-Tone-Terminator Mixer/LO Amplifier **MT3A-0113HCSM**

1. Device Overview

QFN

1.1 General Description

The MT3A-0113HCSM is a versatile, robust, and broadband Two-Tone-Terminator mixer integrated with a low phase noise LO driver amplifier. The MT3A-0113HCSM employs the most sophisticated mixer on the market today and offers unparalleled performance when compared to all other mixer technologies. The MT3A-0113HCSM delivers exceptional IMD suppression with low conversion loss and high IP3. The integrated positive bias only LO amplifier allows for high linearity with LO drive levels down to just +5dBm.

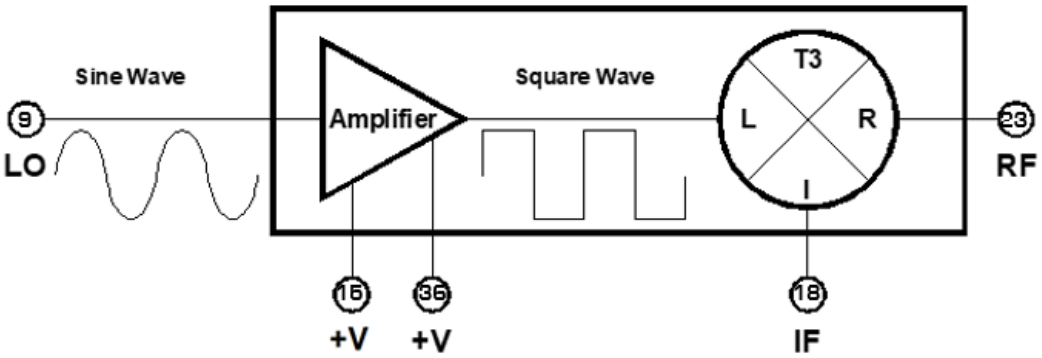
1.2 Features

Parameter	Typical
RF/LO response	1.5GHz - 13GHz
IF response	0.5 – 8.5 GHz
Conversion Loss	9.5 dB
Minimum LO drive	+5dBm

1.3 Applications

- Test and measurement equipment
- SATCOM
- Radar
- Electronic Warfare

1.4 Functional Block Diagram



1.5 Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
MT3A-0113HCSM	6x6 mm QFN	CSM	**RoHS**	Active	EAR99
EVB-MT3A-0113HC	Connectorized Evaluation Fixture	Eval		Active	EAR99

[1] Refer to our website for a list of definitions for terminology presented in this table.

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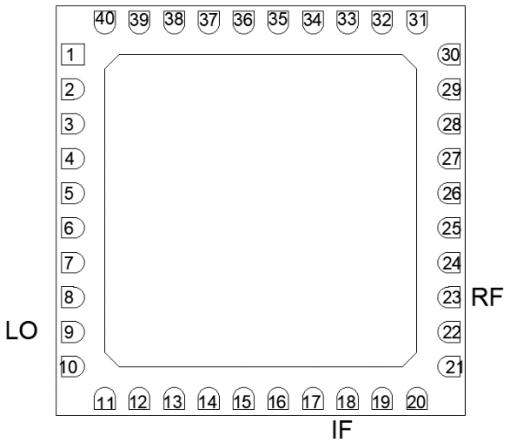
Revision History

Revision Code	Revision Date	Comment
-	October 2021	Datasheet Initial Release

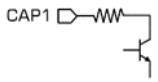
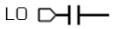
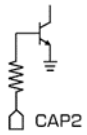
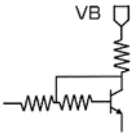
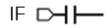
2. Port Configurations and Functions

2.1 Port Diagram

A top-down x-ray view of the MT3A-0113HCSM's CSM Package outline drawing is shown below. The MT3A-0113HCSM has the input and output ports given in Port Functions.



2.2 Port Functions

Port	Function	Description	Equivalent Circuit for Package
Pin 3	Cap 1	Pin 3 allows the user to attach additional off chip bypass capacitance to provide adequate low frequency AC grounding termination to the input matching network. The value should be at least 100nF.	
Pin 9	LO	The LO port is DC blocked and AC matched to 50 Ohms from 1.5 GHz to 13 GHz.	
Pin 13	Cap 2	Pin 13 allows the user to attach additional off chip bypass capacitance to provide adequate low frequency AC grounding termination to the input matching network. The value should be at least 100nF.	
Pin 15	VB	Pin 15 is the DC voltage bias for the current mirror that controls collector current supplied to the amplifier. Larger voltages result in a higher current draw through port VC, effectively functioning as a gain control pin of the amplifier	
Pin 18	IF	Pin 18 is DC blocked and AC matched to 50 Ohms from 500 MHz to 8.5 GHz.	
Pin 23	RF	Pin 23 is DC short to ground and AC matched to 50 Ohms from 1.5 GHz to 13 GHz. Blocking capacitor is optional.	
Pin 38	VC	Pin 38 is the DC voltage supply that supplies the amplifier's collector current.	
GND	Ground	IC backside must be connected to a DC/RF ground with high thermal and electrical conductivity.	

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
DC Voltage on VB or VC	+8	V
DC Bias Current	150	mA
RF Power Handling	+25	dBm
LO Power Handling	+15	dBm
Operating Temperature	-55 to +85	°C
Storage Temperature	-65 to 125	°C
θJC, Junction to Case Thermal Resistance	61	°C/W
Max Junction Temperature for MTTF> 1E6 hours	125	°C
Max Power Dissipation for MTTF of 1E6 hours at 85°C Baseplate Temperature	650	mW

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	1A
Weight	EVAL package	33 g

3.3 Recommended Operating Conditions

The Recommended Operating Conditions indicate the limits, inside which the device should be operated, to guarantee the performance given in Electrical Specifications Operating outside these limits may not necessarily cause damage to the device, but the performance may degrade outside the limits of the electrical specifications. For limits, above which damage may occur, see Absolute Maximum Ratings.

	Min	Nominal	Max	Units
T_A, Ambient Temperature	-55	+25	+85	°C
LO Input Power	+5	+12	+15	dBm
Positive DC Voltage (VC) [2]	+5	+7	+8	V
Positive DC Current Mirror Voltage (VB)	+5	+6	+8	
Current Draw	80	120	150	mA

[2] There is no sequencing required to apply DC or RF power to the mixer.

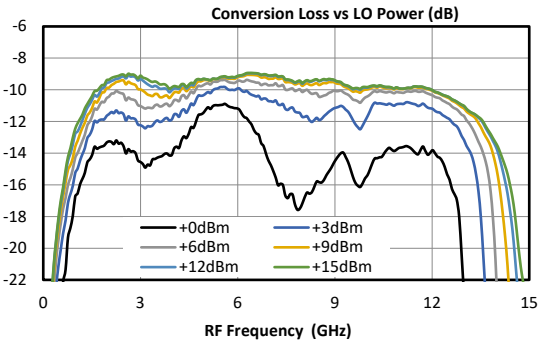
3.5 Electrical Specifications

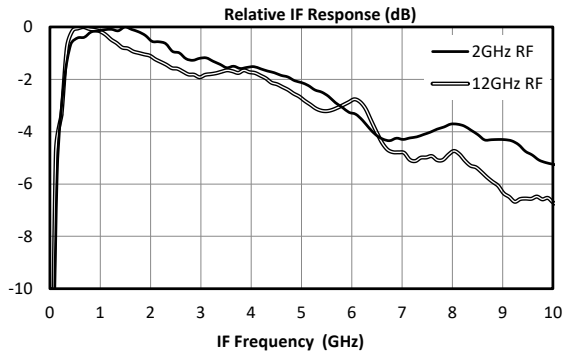
The electrical specifications apply at TA=+25°C in a 50Ω system. Typical data shown is for a down conversion application with a +12dBm sine wave LO input to the integrated LO driver amp biased at +6VB/+7VC.

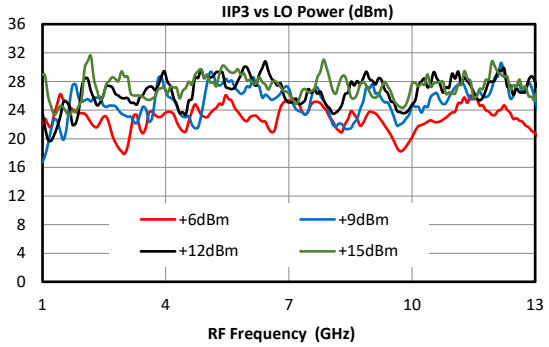
Parameter		Test Conditions	Min	Typical	Max	Units
RF (Pin 23) Frequency Range			1.5		13	GHz
LO (Pin 9) Frequency Range			1.5		13	
I (Pin 18) Frequency Range			0.5		8.5	
Conversion Loss (CL)[3]		RF/LO = 1.5 - 13 GHz I = 0.5 - 2 GHz		9.5	14	dB
		RF/LO = 1.5 - 13 GHz I = 2 – 8.5 GHz		11.5		
Noise Figure (NF)[4]		RF/LO = 1.5 - 13 GHz I = 0.5 - 2 GHz		10		dB
RF to IF Isolation		RF/IF = 1.5 - 13 GHz		See Plot		dBm
LO Leakage	LO to IF	IF/LO = 1.5 - 13 GHz		See Plot		
	LO to RF	RF/LO = 1.5 - 13 GHz		See Plot		
Input IP3 (IIP3)		RF/LO = 1.5 - 13 GHz I = 0.5 - 2 GHz		28		dBm
Input 0.1 dB Gain Compression Point (P0.1dB)				+13		dBm
Bias Requirements (mA) +6.0VB/+7.0VC			80	120	150	mA

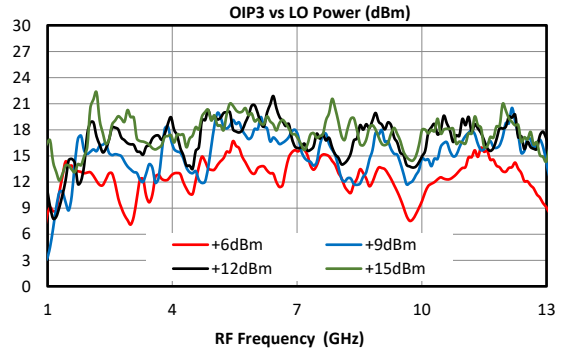
[3] Measured as a down converter to a fixed 1 GHz IF.
[4] Mixer Noise Figure typically measures within 0.5 dB of conversion loss for IF frequencies greater than 5 MHz.

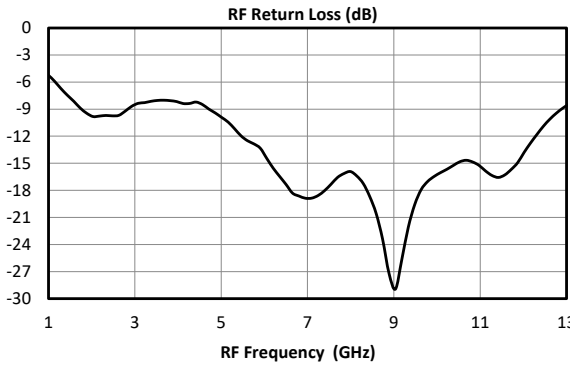
3.6 Typical Performance Plots

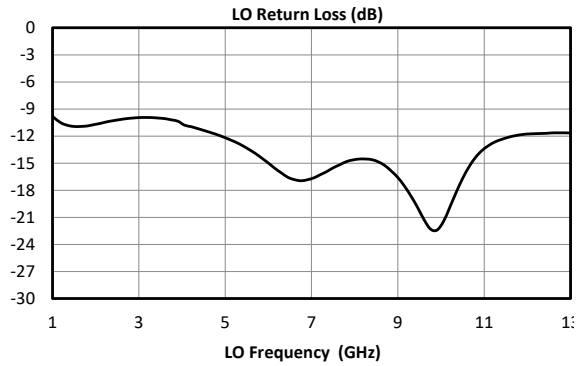


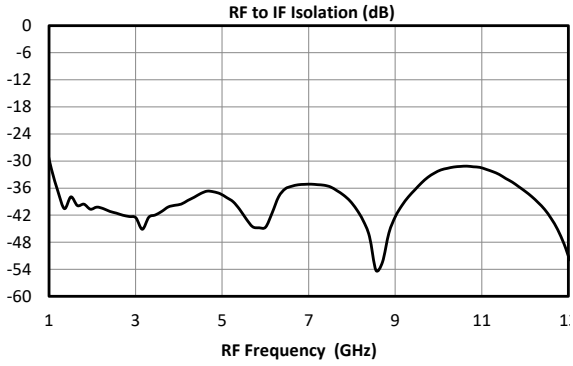


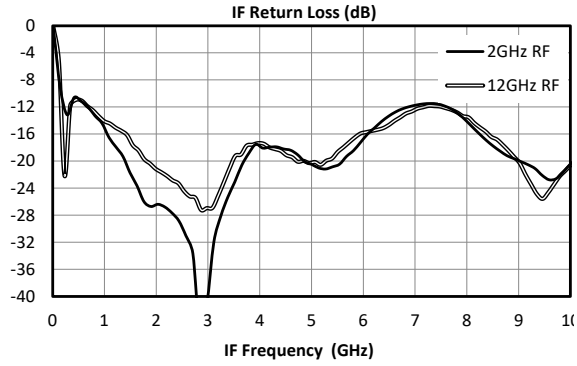


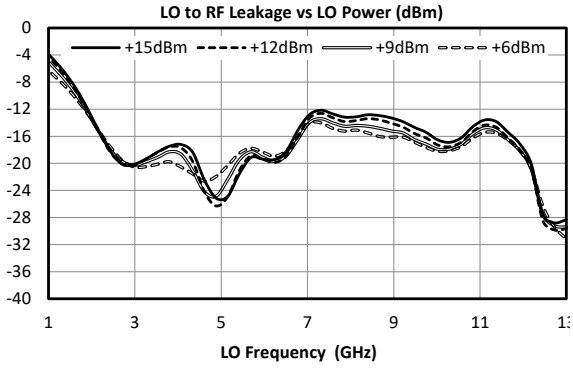


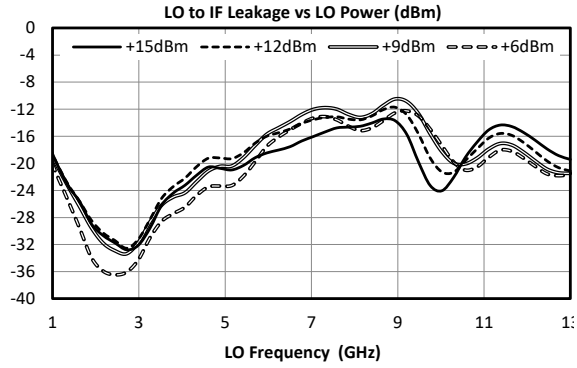


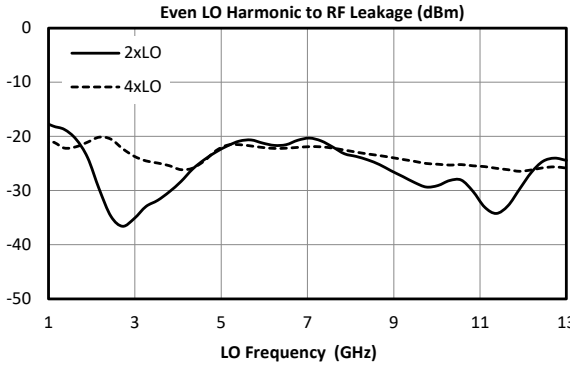


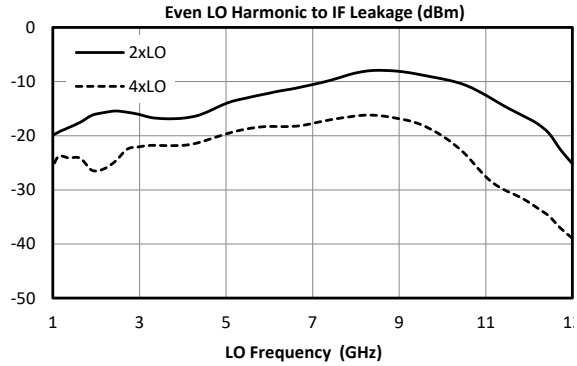


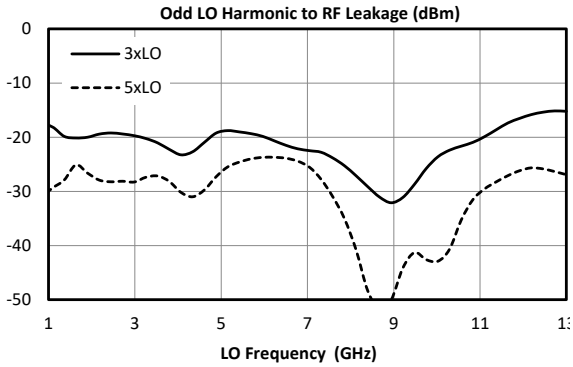


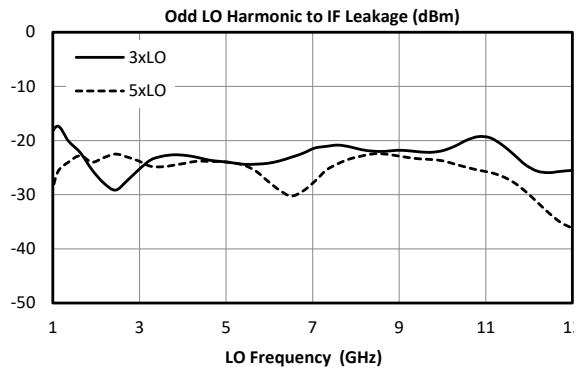


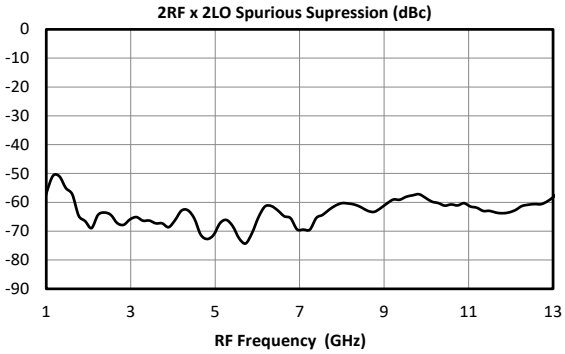


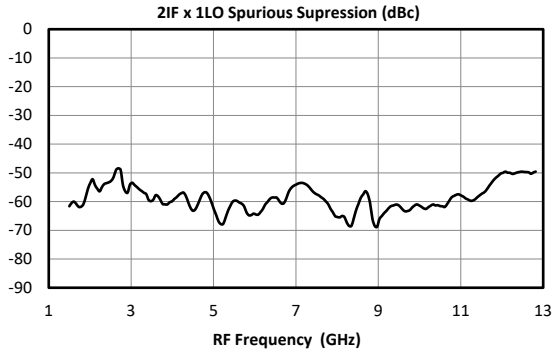












3.6.1 Typical Spurious Performance: Down-Conversion

Typical spurious data is provided by selecting RF and LO frequencies (± m*LO ± n*RF) within the RF/LO bands, to create a spurious output within the IF band. The mixer is swept across the full spurious band and the mean is calculated. The numbers shown in the table below are for a -10 dBm RF input. Spurious suppression is scaled for different RF power levels by (n-1), where "n" is the RF spur order. For example, the 2RF x 2LO spur is 63 dBc for a -10 dBm input, so a -20 dBm RF input creates a spur that is (2-1) x (-10 dB) lower, or 73 dBc. Data is shown for the frequency plan in 3.6 Typical Performance. mLOx0RF plots can be found in section 3.6.2 . 0LOx1RF plot is identical to the plot of LO-RF isolation.

Typical Down-conversion spurious suppression (dBc)

-10 dBm RF Input	0xLO	1xLO	2xLO	3xLO	4xLO	5xLO
1xRF	23	Reference	21	18	18	20
2xRF	64	65	63	41	63	62
3xRF	95	81	57	80	83	84
4xRF	103	115	111	112	112	112
5xRF	128	132	129	129	129	129

3.6.2 Typical Spurious Performance: Up-Conversion

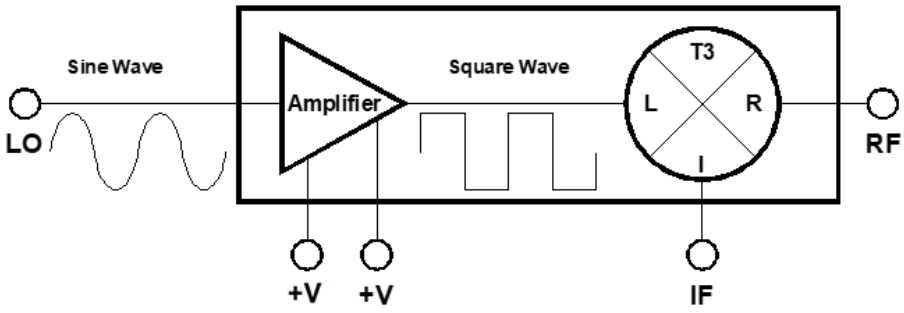
Typical spurious data is taken by mixing an input within the IF band, with LO frequencies (± m*LO ± n*IF), to create a spurious output within the RF output band. The mixer is swept across the full spurious output band and the mean is calculated. The numbers shown in the table below are for a -10 dBm IF input. Spurious suppression is scaled for different IF input power levels by (n-1), where "n" is the IF spur order. For example, the 2IFx1LO spur is typically 63 dBc for a -10 dBm input with a sine-wave LO, so a -20 dBm IF input creates a spur that is (2-1) x (-10 dB) lower, or 73 dBc. Data is shown for the frequency plan in 3.6 Typical Performance.

Typical Up-conversion spurious suppression (dBc)

-10 dBm IF Input	0xLO	1xLO	2xLO	3xLO	4xLO	5xLO
1xIF	22	Reference	20	18	18	24
2xIF	67	63	66	41	63	53
3xIF	92	81	56	78	75	73
4xIF	116	109	114	107	108	101
5xIF	127	124	127	120	123	118

4. Operation

4.1 Application Circuit Block Diagram



See T3 Mixer Primer for benefits of square wave LO drive with T3 mixers

4.2 Ports Operation

IF Port – Used as input on an upconversion, output on downconversion, or LO port in a band shifting application. Signals should be connected by 50 ohm microstrip or coplanar traces to well matched broadband 50 ohm sources and loads.

RF Port – Used as input on a downconversion, output on upconversion, or output in a band shifting application. Signals should be connected by 50 ohm microstrip or coplanar traces to well matched broadband 50 ohm sources and loads.

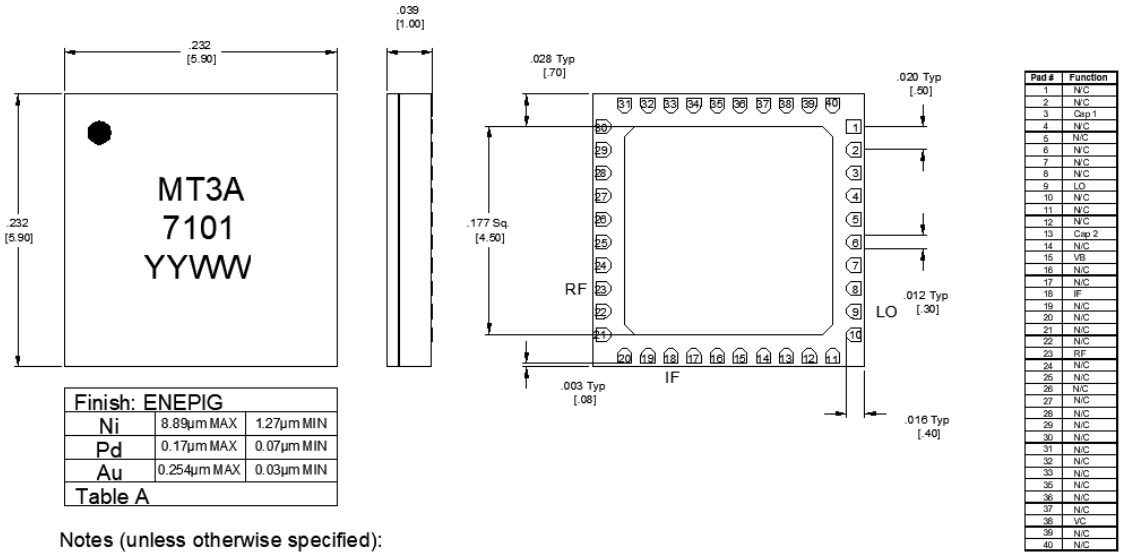
LO Port – The noise floor of the LO input signal should be less than the value of the noise floor plus isolation of the mixer, or a filter is recommended to prevent reduction in dynamic range. An integrated LO amplifier is included, allowing for superior performance with LO power below the typical recommended drive level.

Filtering and Matching- Filtering is generally desired for spurious and image removal on the output port of the mixer. Reflective filters can cause out of band signals to reflect back into the mixer and cause conversion loss ripple, erroneous spurs, and other undesired behaviors. To eliminate these problems it is recommend that the filters be placed as close to the output port as possible. If undesired behavior is still observed, a diplexer with one port terminated or a 1-3 dB attenuator may reduce this problem.

RF Ground – The ground paddle of the QFN should be connected to a low noise RF ground with very low electrical resistance for high frequency operation.

5. Mechanical Data

5.1 CSM Package Outline Drawing



Finish: ENEPIG		
Ni	8.89µm MAX	1.27µm MIN
Pd	0.17µm MAX	0.07µm MIN
Au	0.254µm MAX	0.03µm MIN
Table A		

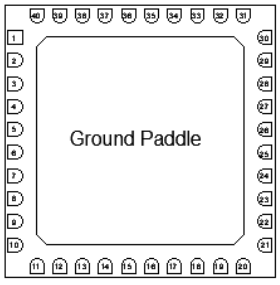
Pad #	Function
1	N/C
2	N/C
3	Cap 1
4	N/C
5	N/C
6	N/C
7	N/C
8	N/C
9	LO
10	N/C
11	N/C
12	N/C
13	Cap 2
14	N/C
15	VB
16	N/C
17	N/C
18	IF
19	N/C
20	N/C
21	N/C
22	N/C
23	RF
24	N/C
25	N/C
26	N/C
27	N/C
28	N/C
29	N/C
30	N/C
31	N/C
32	N/C
33	N/C
35	N/C
36	N/C
37	N/C
38	VC
39	N/C
40	N/C

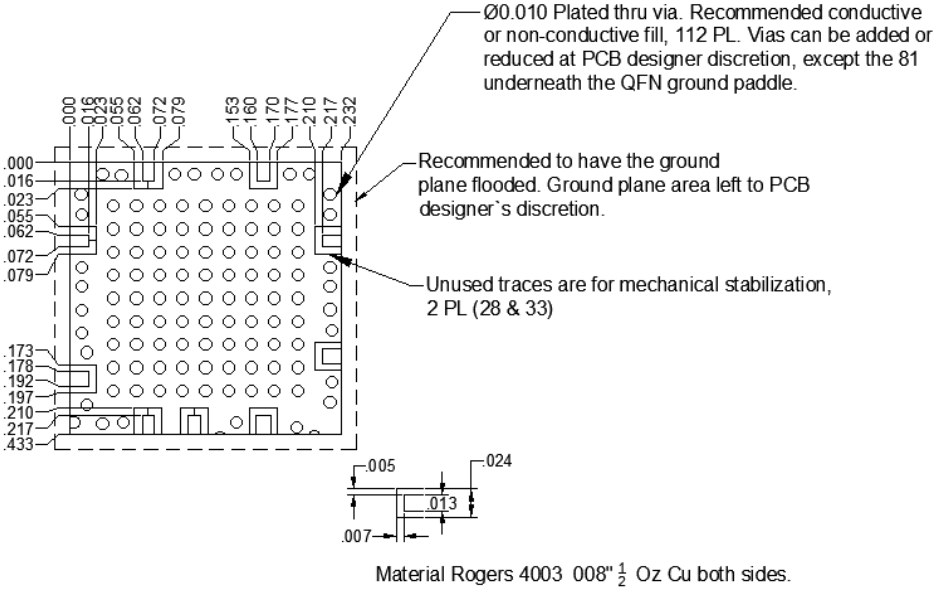
Notes (unless otherwise specified):

1. Substrate material is Ceramic.
2. All unconnected pins should be connected to PCB RF ground.

5.2 CSM Package Footprint

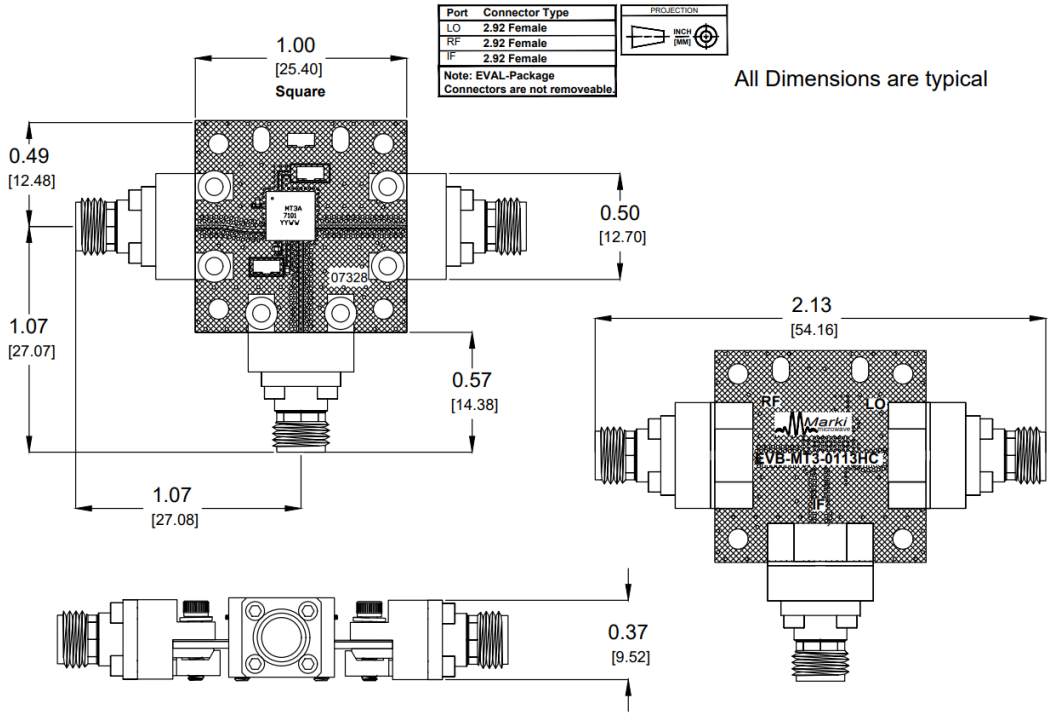
QFN 6mm Plastic Sample Drawing
X-Ray view



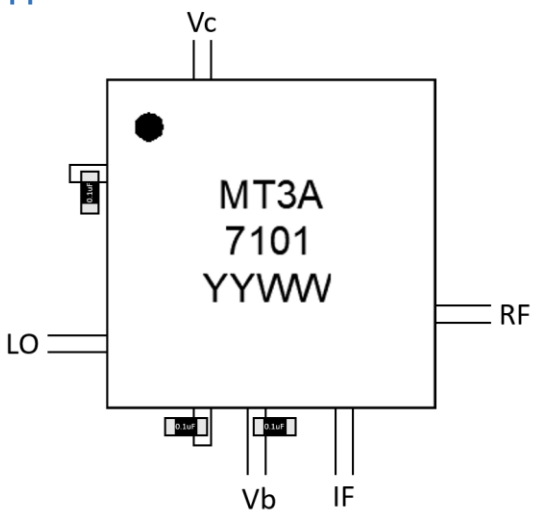


QFN-Package Surface-Mount Landing Pattern
Click here for a DXF of the above layout.
Click here for leaded solder reflow. Click here for lead-free solder reflow.

5.3 Evaluation Board Outline Drawing



5.4 Evaluation Board Application Circuit



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